74HC594; 74HCT594

8-bit shift register with output register

Rev. 8 — 19 March 2023 Product data sheet

1. General description

The 74HC594; 74HCT594 is an 8-bit serial-in/serial or parallel-out shift register with a storage register. Separate clock and reset inputs are provided on both shift and storage registers. The device features a serial input (DS) and a serial output (Q7S) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the SHCP input, and the data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. A LOW level on one of the two register reset pins ($\overline{SHR}$ and $\overline{STR}$) will clear the corresponding register. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Synchronous serial input and output
- 8-bit parallel output
- Shift and storage registers have independent direct clear and clocks
- Independent clocks for shift and storage registers
- 100 MHz (typical)
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC594: CMOS level
  - For 74HCT594: TTL level
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Serial-to parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC594D 74HCT594D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC594DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC594PW 74HCT594PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC594BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

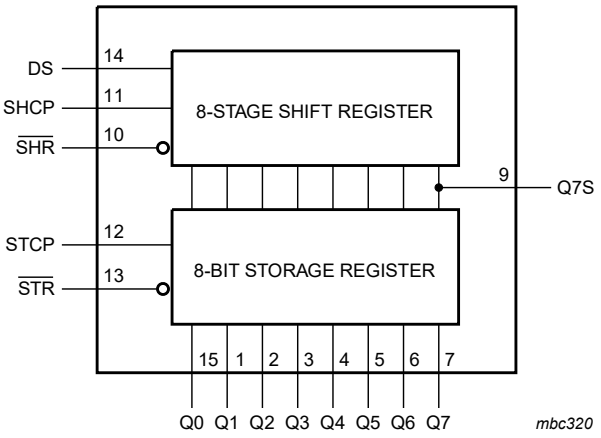


Fig. 1. Functional diagram

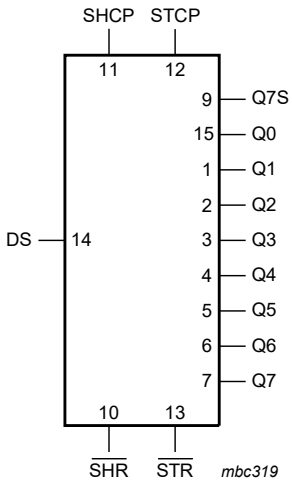


Fig. 2. Logic symbol

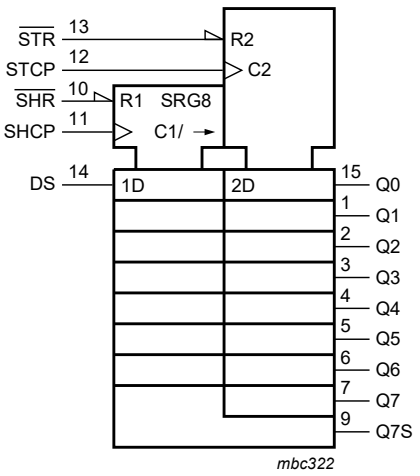


Fig. 3. IEC logic symbol

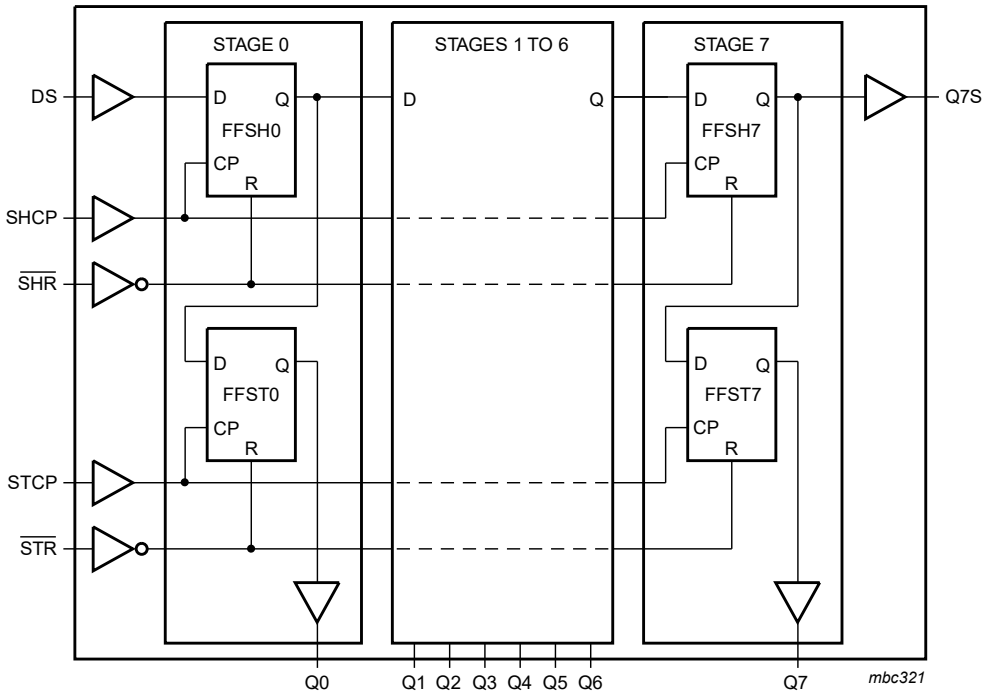


Fig. 4. Logic diagram

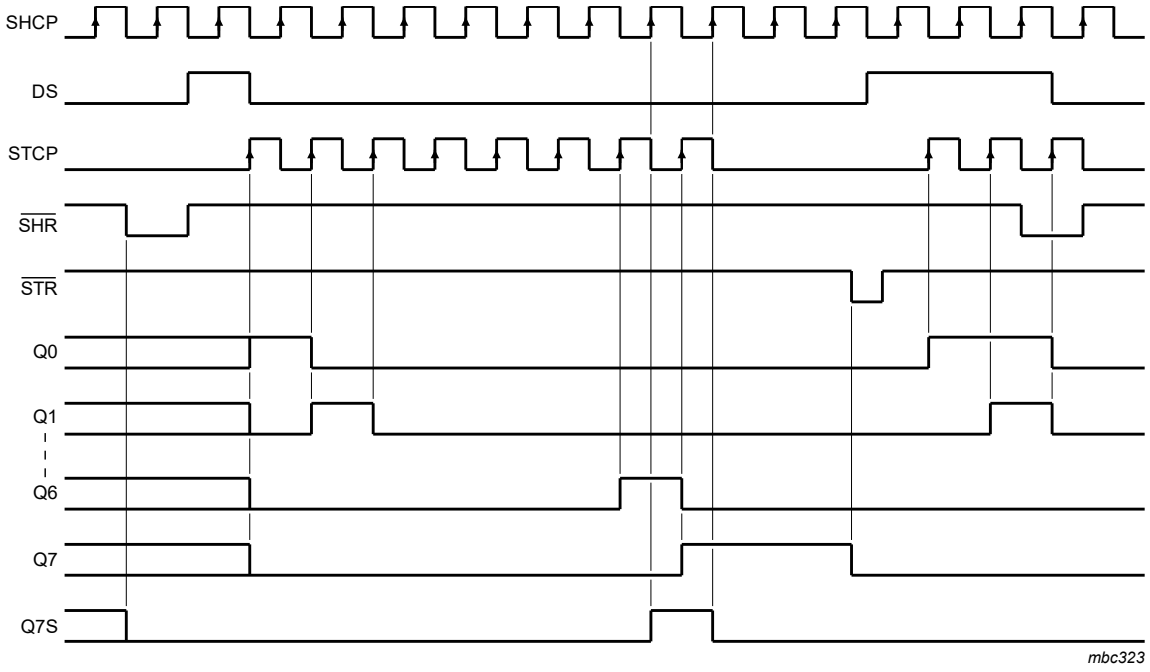
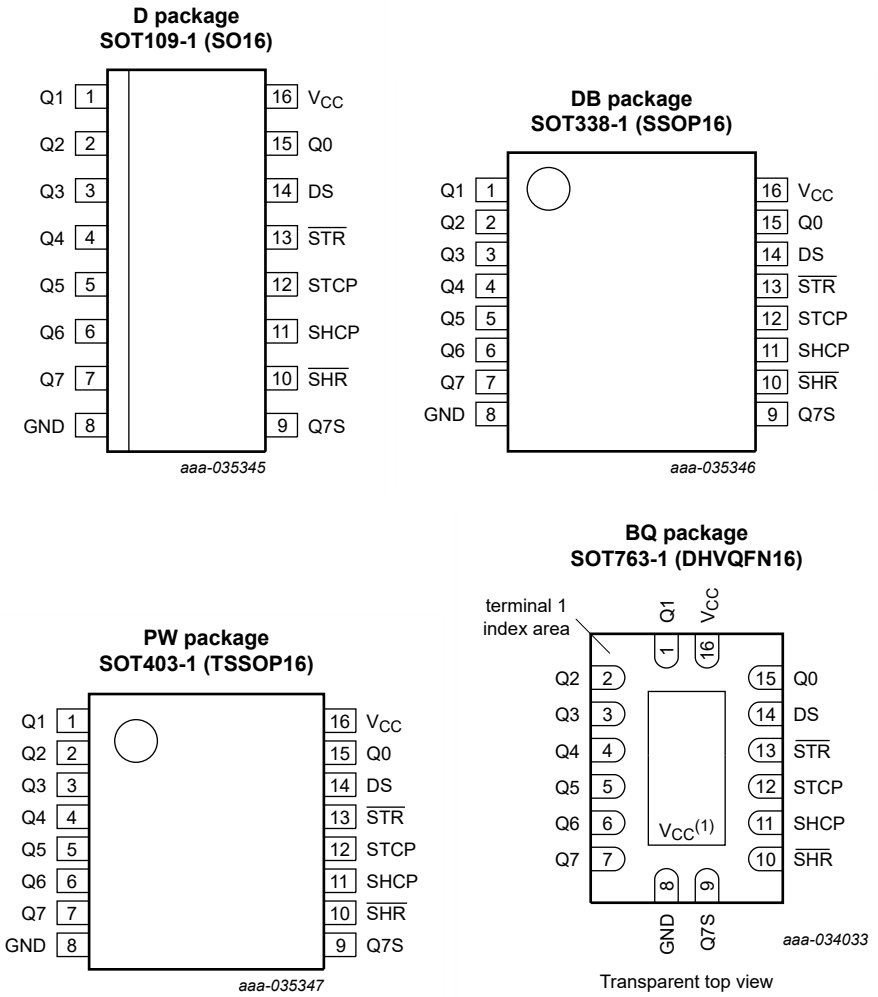


Fig. 5. Timing diagram

6. Pinning information

6.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{SHR}$	10	shift register reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{STR}$	13	storage register reset (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition; X = don't care.

Function	Input				
	$\overline{SHR}$	$\overline{STR}$	SHCP	STCP	DS
Clear shift register	L	X	X	X	X
Clear storage register	X	L	X	X	X
Load DS into shift register stage 0, advance previous stage data to the next stage	H	X	↑	X	H or L
Transfer shift register data to storage register and outputs Qn	X	H	X	↑	X
Shift register one count pulse ahead of storage register	H	H	↑	↑	X

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V				
		Serial data output Q7S		-	±25	mA
		Parallel data output Qn		-	±35	mA
I_{CC}	supply current	Serial data output Q7S		-	50	mA
		Parallel data output Qn		-	70	mA
I_{GND}	ground current	Serial data output Q7S		-	-50	mA
		Parallel data output Qn		-	-70	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC594			74HCT594			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics type 74HC594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		Q7S; I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		Qn; I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		Q7S; I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		Qn; I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		Q7S; I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		Qn; I_O = -7.8 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		Q7S; I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		Qn; I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		Q7S; I_O = -5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		Qn; I_O = -7.8 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		Q7S; I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		Qn; I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

Table 7. Static characteristics type 74HCT594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V and other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pins $\overline{SHR}$, SHCP, STCP, $\overline{STR}$	-	150	540	µA
		pin DS	-	25	90	µA
C_i	input capacitance		-	3.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V and other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pins $\overline{SHR}$, SHCP, STCP, $\overline{STR}$	-	-	675	µA
		pin DS	-	-	112.5	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = -4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		Qn; I_O = -6.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		Q7S; I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		Qn; I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V and other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pins $\overline{SHR}$, SHCP, STCP, $\overline{STR}$	-	-	735	µA
		pin DS	-	-	122.5	µA

11. Dynamic characteristics

Table 8. Dynamic characteristics type 74HC594

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; For test circuit see Fig. 12.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [1]								
		V_{CC} = 2.0 V	-	44	150	-	185	-	225	ns
		V_{CC} = 4.5 V	-	16	30	-	37	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	31	-	38	ns
		STCP to Qn; see Fig. 7								
		V_{CC} = 2.0 V	-	44	150	-	185	-	225	ns
		V_{CC} = 4.5 V	-	16	30	-	37	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	31	-	38	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{SHR}$ to Q7S; see Fig. 10								
		V_{CC} = 2.0 V	-	39	150	-	185	-	225	ns
		V_{CC} = 4.5 V	-	14	30	-	37	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	26	-	31	-	38	ns
		$\overline{STR}$ to Qn; see Fig. 11								
		V_{CC} = 2.0 V	-	39	125	-	155	-	185	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	37	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	21	-	26	-	31	ns
t_{THL}	HIGH to LOW output transition time	Q7S; see Fig. 6								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
		Qn								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t_{TLH}	LOW to HIGH output transition time	Q7S; see Fig. 6								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
		Qn								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	SHCP (HIGH or LOW); see Fig. 6								
		V_{CC} = 2.0 V	80	10	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		STCP (HIGH or LOW); see Fig. 7								
		V_{CC} = 2.0 V	80	10	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		$\overline{SHR}$ and $\overline{STR}$ (HIGH or LOW); see Fig. 10 and Fig. 11								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 8								
		V_{CC} = 2.0 V	100	10	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	4	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	3	-	21	-	26	-	ns
		$\overline{SHR}$ to STCP; see Fig. 9								
		V_{CC} = 2.0 V	100	14	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	5	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	4	-	21	-	26	-	ns
		SHCP to STCP; see Fig. 7								
		V_{CC} = 2.0 V	100	17	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	6	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	5	-	21	-	26	-	ns
t_h	hold time	DS to SHCP; see Fig. 8								
		V_{CC} = 2.0 V	25	-8	-	30	-	35	-	ns
		V_{CC} = 4.5 V	5	-3	-	6	-	7	-	ns
		V_{CC} = 6.0 V	4	-2	-	5	-	6	-	ns
t_{rec}	recovery time	$\overline{SHR}$ to SHCP and $\overline{STR}$ to STCP; see Fig. 10 and Fig. 11								
		V_{CC} = 2.0 V	50	-14	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	-5	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	-4	-	11	-	13	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	SHCP or STCP; see Fig. 6 and Fig. 7								
		V_{CC} = 2.0 V	6.0	30	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	92	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	100	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	109	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [2]	-	84	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics type 74HCT594

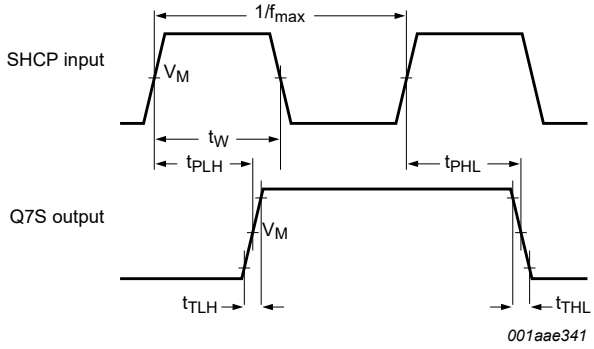
GND = 0 V; V_{CC} = 4.5 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; For test circuit see Fig. 12.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [1]	-	18	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		STCP to Qn; see Fig. 7	-	18	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{SHR}$ to Q7S; see Fig. 10	-	17	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		$\overline{STR}$ to Qn; see Fig. 11	-	17	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
t_{THL}	HIGH to LOW output transition time	Q7S; see Fig. 6								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		Qn								
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
t_{TLH}	LOW to HIGH output transition time	Q7S; see Fig. 6								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		Qn								
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
t_W	pulse width	SHCP (HIGH or LOW); see Fig. 6	16	4	-	20	-	24	-	ns
		STCP (HIGH or LOW); see Fig. 7	16	4	-	20	-	24	-	ns
		$\overline{SHR}$ and $\overline{STR}$ (HIGH or LOW); see Fig. 10 and Fig. 11	16	6	-	20	-	24	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	DS to SHCP; see Fig. 8	20	4	-	25	-	30	-	ns
		$\overline{SHR}$ to STCP; see Fig. 9	20	6	-	25	-	30	-	ns
		SHCP to STCP; see Fig. 7	20	7	-	25	-	30	-	ns
t_h	hold time	DS to SHCP; see Fig. 8	5	-3	-	6	-	7	-	ns
t_{rec}	recovery time	$\overline{SHR}$ to SHCP and $\overline{STR}$ to STCP; see Fig. 10 and Fig. 11	10	-5	-	13	-	15	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Fig. 6 and Fig. 7	30	92	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	100	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V; V_{CC} = 5 V; f_i = 1 MHz [2]	-	89	-	-	-	-	-	pF

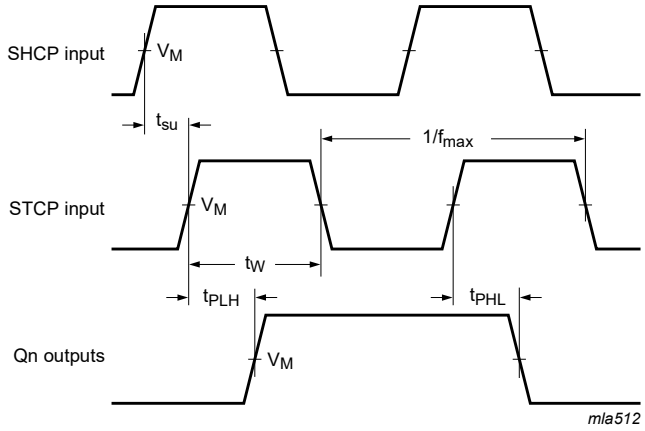
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



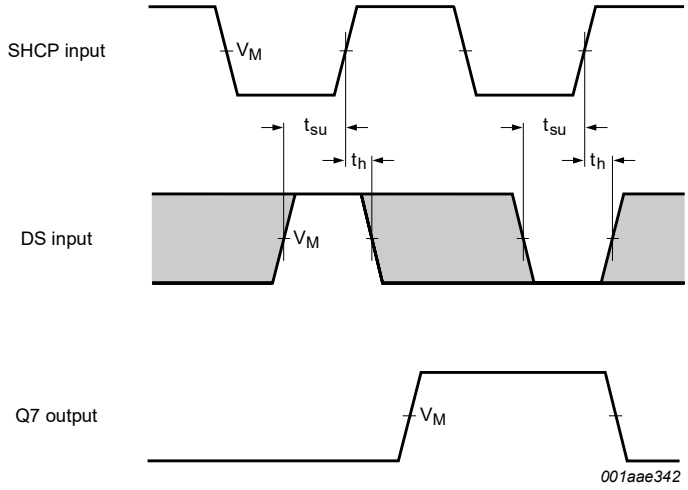
Measurement points are given in Table 10.

Fig. 6. The shift clock (SHCP) to output (Q7S) propagation delays, the shift clock pulse width, the maximum shift clock frequency, and output transition times



Measurement points are given in Table 10.

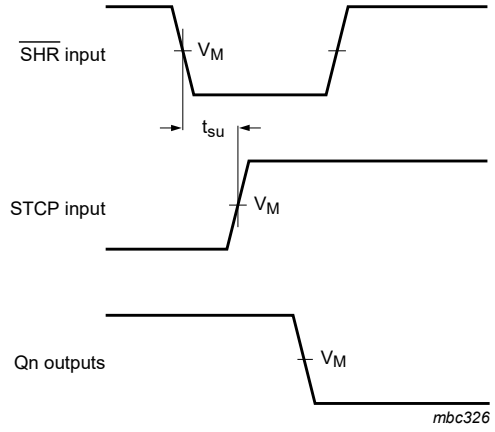
Fig. 7. The storage clock (STCP) to output (Qn), propagation delays, the storage clock pulse width, the maximum storage clock pulse frequency and the shift clock to storage clock set-up time



Measurement points are given in Table 10.

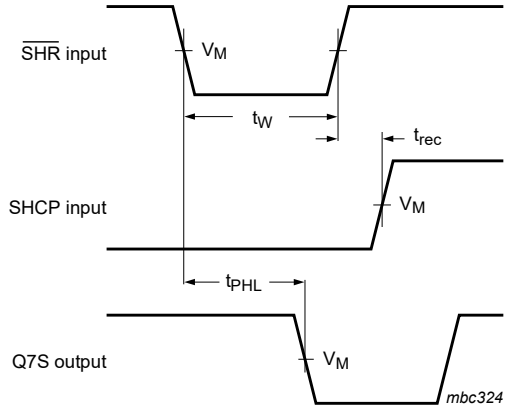
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. The data set-up time and hold times for DS input to SHCP



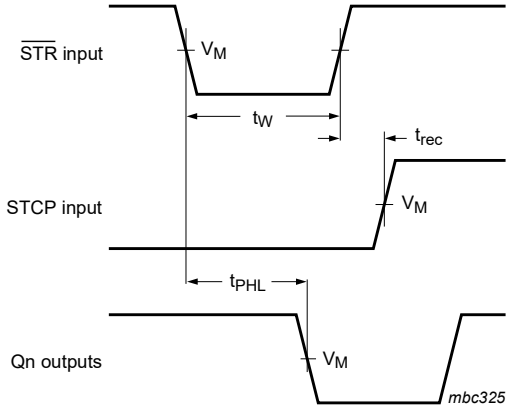
Measurement points are given in Table 10.

Fig. 9. The set-up time shift reset ($\overline{SHR}$) to storage clock (STCP)



Measurement points are given in Table 10.

Fig. 10. The shift reset (SHR) pulse width, the shift reset to output (Q7S) propagation delay and the shift reset to shift clock (SHCP) recovery time

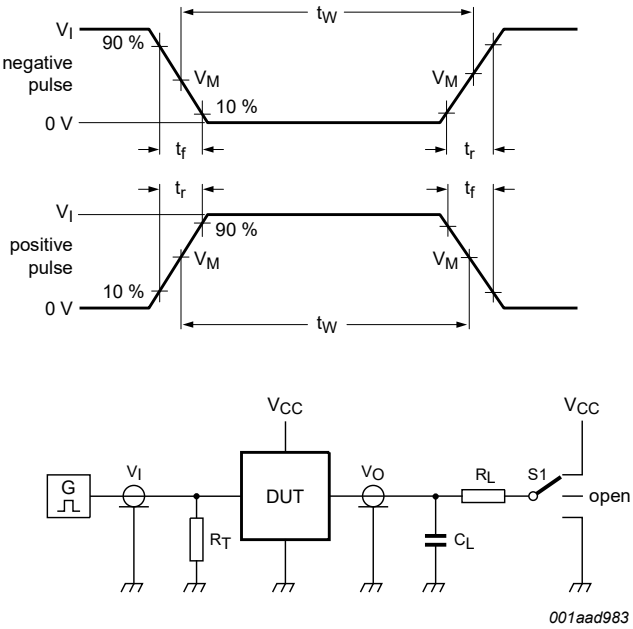


Measurement points are given in Table 10.

Fig. 11. The storage reset (STR) pulse width, the storage reset to output (Qn) propagation delay and the storage reset to storage clock (STCP) recovery time

Table 10. Measurement points

Type	Input	Output
	V_M	V_M
74HC594	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT594	1.3 V	1.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

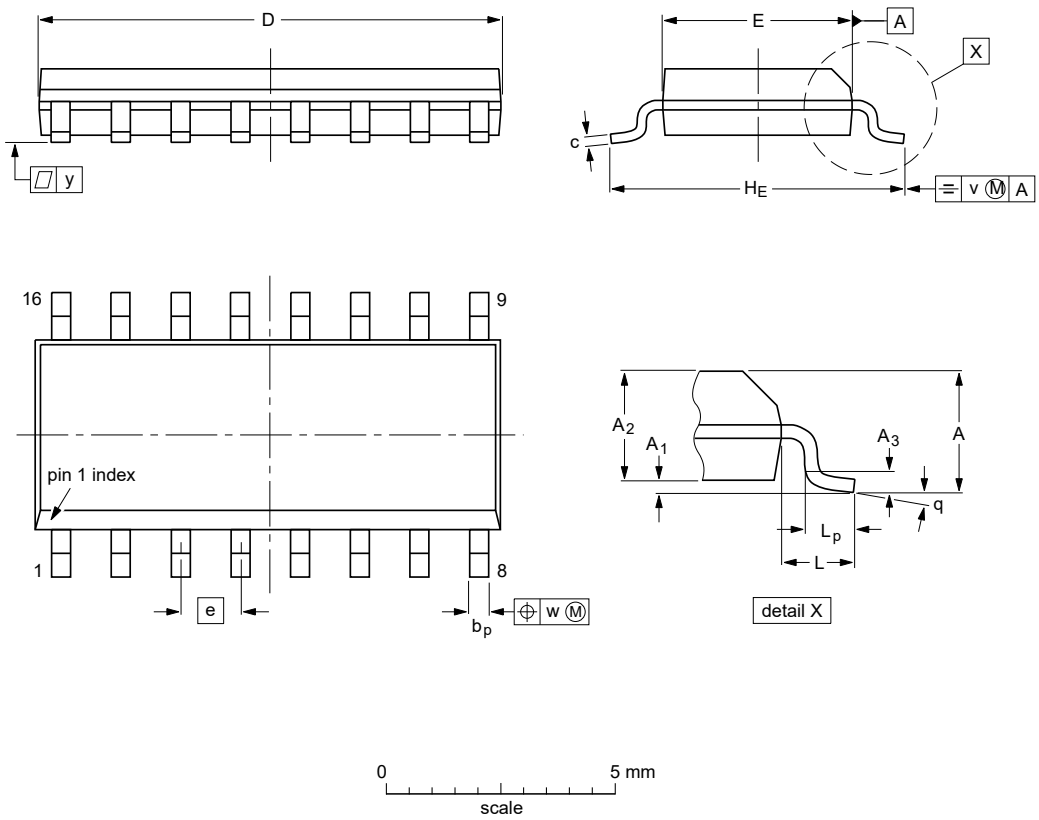
Fig. 12. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC594	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT594	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

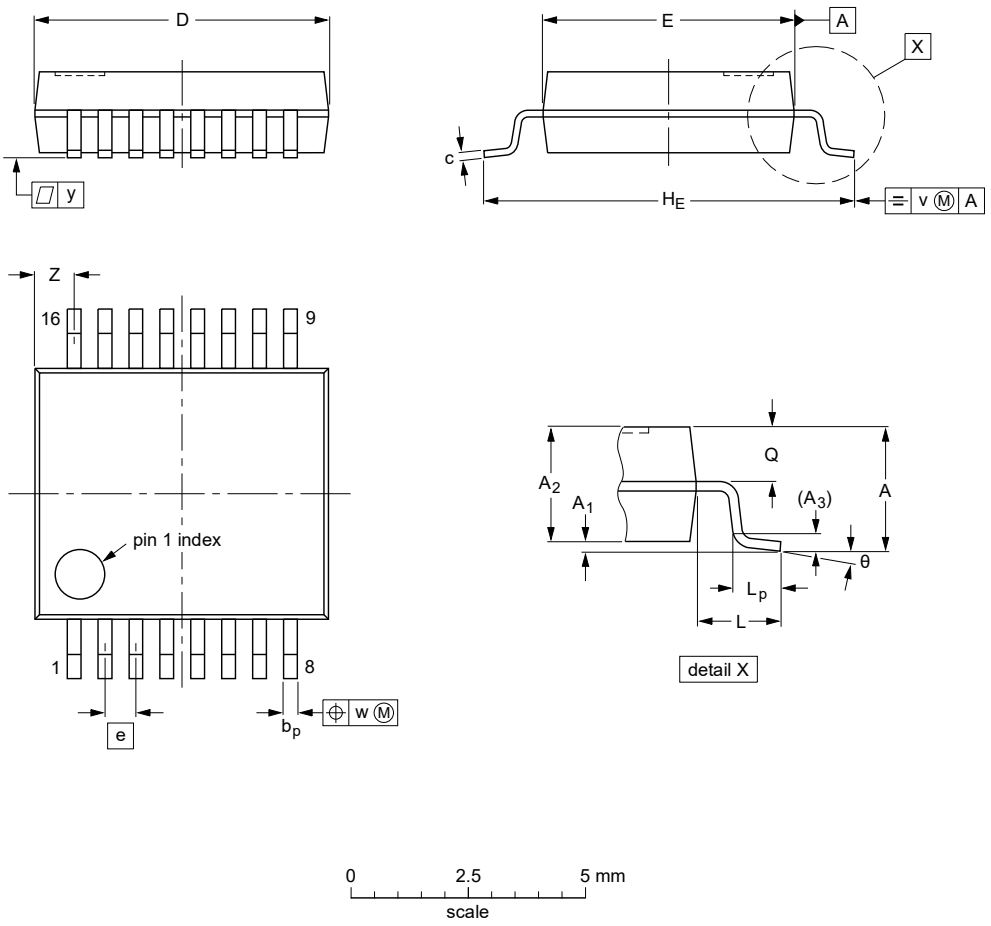
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

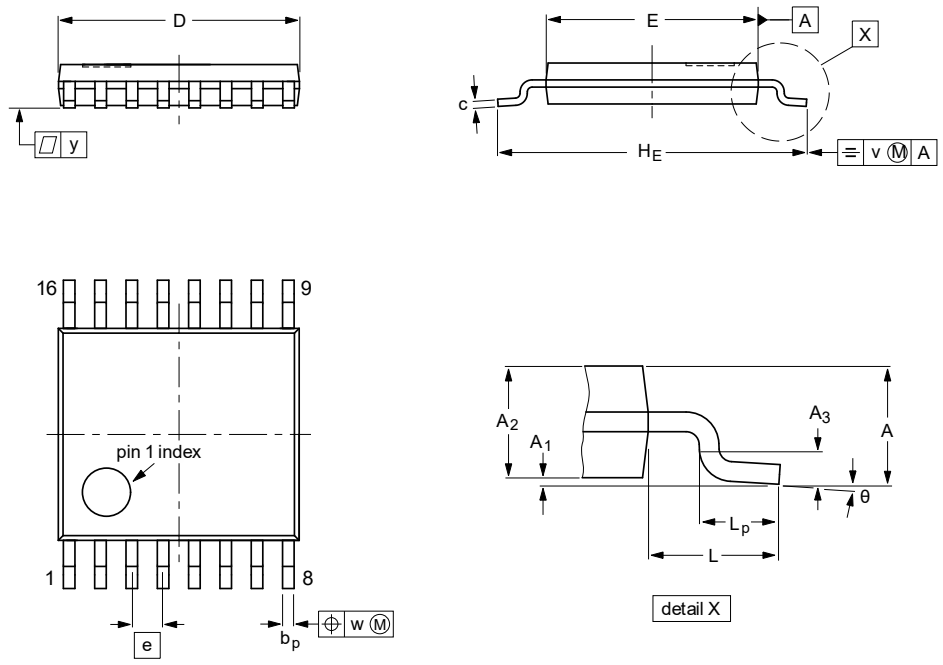
Note

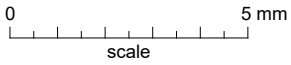
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note

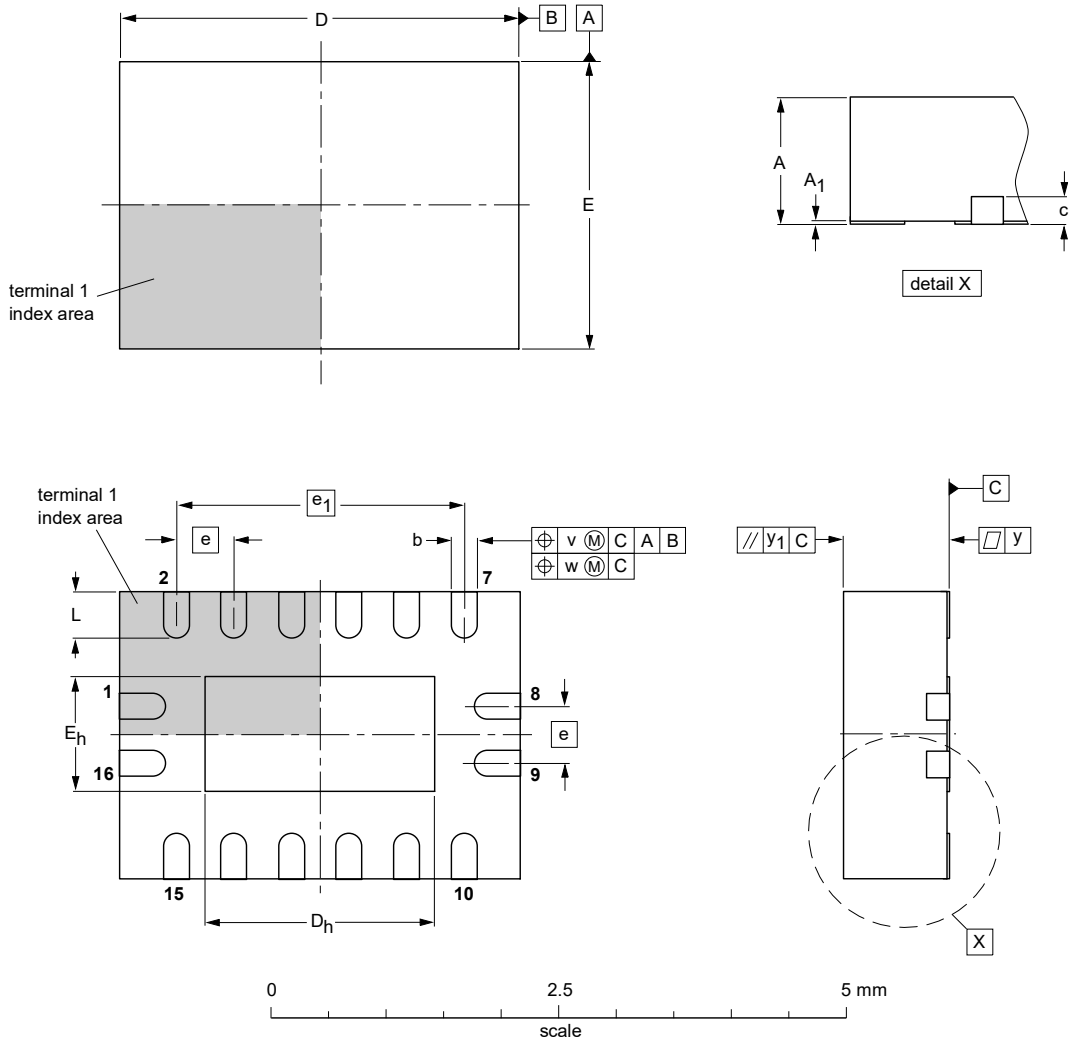
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 16. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT594 v.8	20240319	Product data sheet	-	74HC_HCT594 v.7
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 13 and Fig. 15: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74HC_HCT594 v.7	20221020	Product data sheet	-	74HC_HCT594 v.6
Modifications:	• Type number 74HC594BQ (SOT763-1/DHVQFN16) added.			
74HC_HCT594 v.6	20211022	Product data sheet	-	74HC_HCT594 v.5
Modifications:	• Type number 74HCT594PW (SOT403-1/TSSOP16) added.			
74HC_HCT594 v.5	20210812	Product data sheet	-	74HC_HCT594 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC594PW (SOT403-1/TSSOP16) added. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT594 v.4	20160225	Product data sheet	-	74HC_HCT594 v.3
Modifications:	• Type numbers 74HC594N and 74HCT594N (SOT38-4) removed.			
74HC_HCT594 v.3	20061220	Product data sheet	-	74HC_HCT594_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 1: Ordering information updated.			
74HC_HCT594_CNV v.2	19970908	Product specification	-	74HC_HCT594_CNV v.1

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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