PRELIMINARY DATA

8-STAGE STATIC SHIFT REGISTERS: 4014B-SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT 4021B-ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/ SERIAL OUTPUT

- MEDIUM-SPEED OPERATION-12 MHz (TYP.) CLOCK RATE AT V_{DD}-V_{SS}= 10V
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING AND CONTROL GATING
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4014B, HCC 4021B** (extended temperature range) and the **HCF 4014B, HCF 4021B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4014B** and **HCC/HCF 4021B** series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop in addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the **HCC/HCF 4014B**. In the **HCC/HCF 4021B** serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the **HCC/HCF 4021B**, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple package is permitted.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

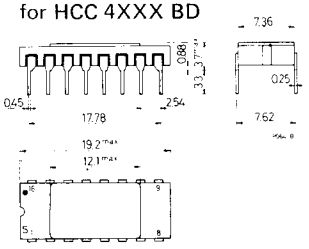
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

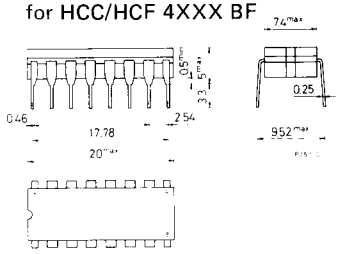
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

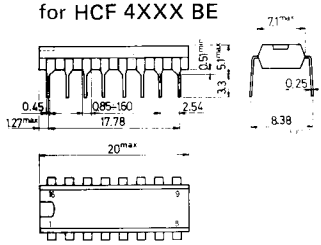
Dual in-line ceramic package for HCC 4XXX BD



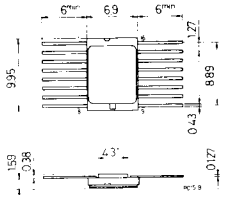
Dual in-line ceramic package for HCC/HCF 4XXX BF



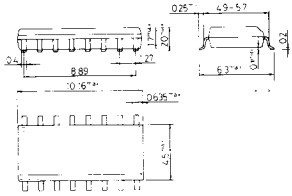
Dual in-line plastic package for HCF 4XXX BE



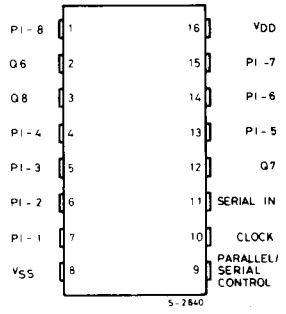
Ceramic flat package for HCC 4XXX BK



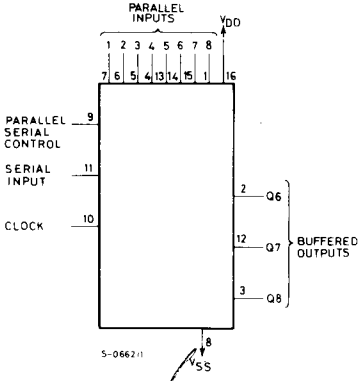
Plastic micropackage for HCF 4XXX BM



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

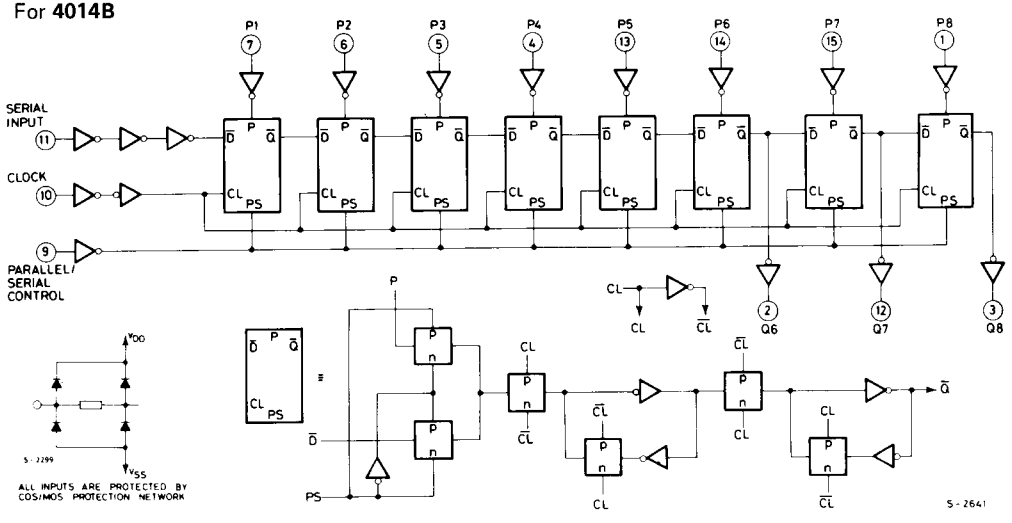


RECOMMENDED OPERATING CONDITIONS

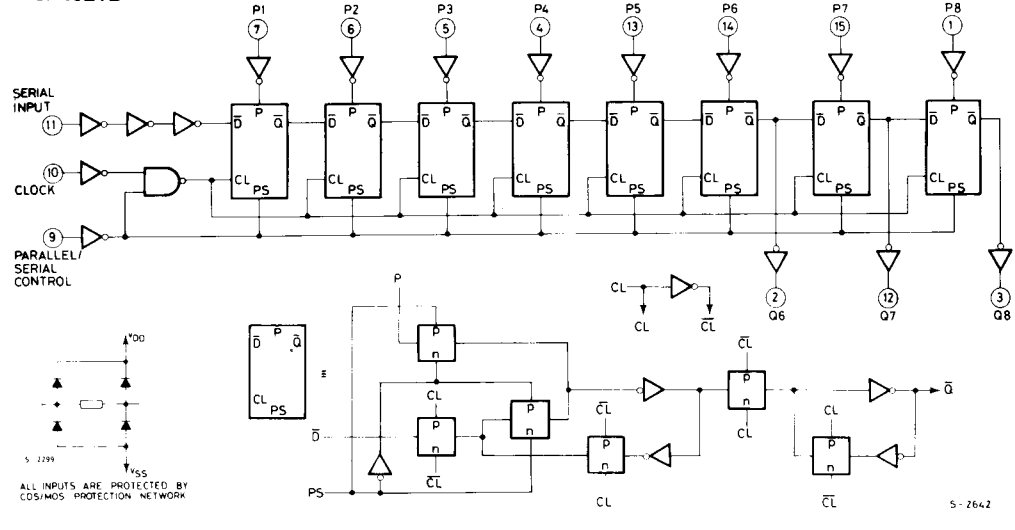
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAMS

For **4014B**



For **4021B**



TRUTH TABLES

For **4014B**

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
⌐‾	X	1	0	0	0	0	
⌐‾	X	1	1	0	1	0	
⌐‾	X	1	0	1	0	1	
⌐‾	X	1	1	1	1	1	
⌐‾	0	0	X	X	0	Q_n-1	
⌐‾	1	0	X	X	1	Q_n-1	
‾⌐	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE
NC = NO CHANGE

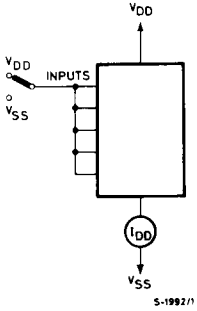
For **4021B**

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐‾	0 1	0 0	X X	X X	0 1	Q_n-1 Q_n-1	
‾⌐	X	0	X	X	Q_1	Q_n	NC

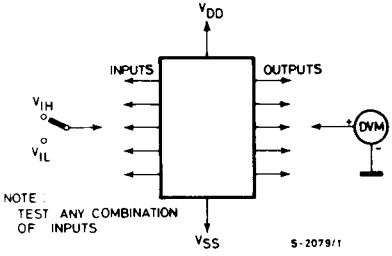
X = DON'T CARE CASE
NC = NO CHANGE

TEST CIRCUITS

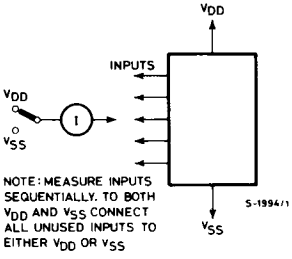
Quiescent device current



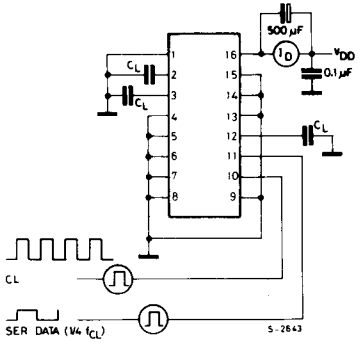
Noise immunity



Input leakage current



Dynamic power dissipation



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

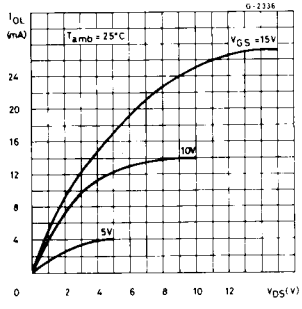
* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

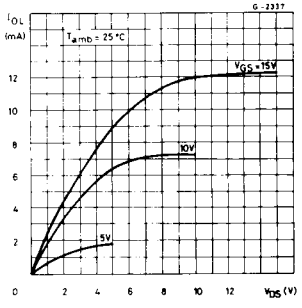
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time	5		160	320	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}*	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8.5	17		
t_W	Clock pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{setup}	Setup time, serial input (ref. to CL)	5	120	60		ns
		10	80	40		
		15	60	30		
t_{setup}	Setup time, parallel inputs (4014B) (ref. to CL)	5	80	40		ns
		10	50	25		
		15	40	20		
t_{setup}	Setup time, parallel inputs (4021B) (ref. to CL)	5	50	25		ns
		10	30	15		
		15	20	10		
t_{setup}	Setup time, parallel/serial control (4014B) (ref. to CL)	5	180	90		ns
		10	80	40		
		15	60	30		
t_{hold}	Hold time, serial in, parallel in, parallel/serial control	5	0			ns
		10	0			
		15	0			
t_{WH}	P/S Pulse width (4021B)	5	160	80		ns
		10	80	40		
		15	50	25		
t_{rem}	P/S Removal, time (4021B) (ref. to CL)	5	280	140		ns
		10	140	70		
		15	100	50		

* If more then one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

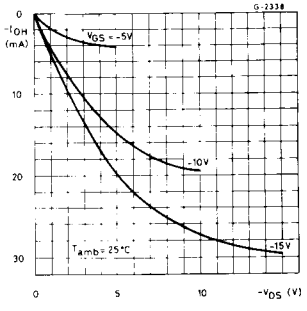
Typical output low (sink) current characteristics



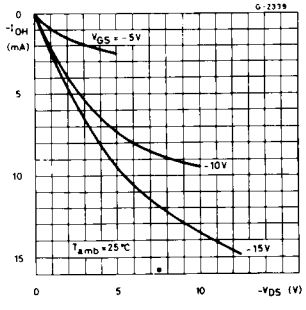
Minimum output low (sink) current characteristics



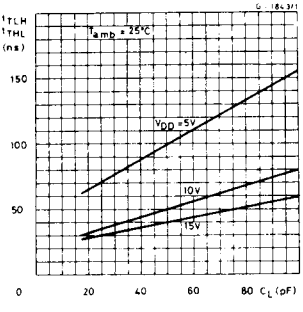
Typical output high (source) current characteristics



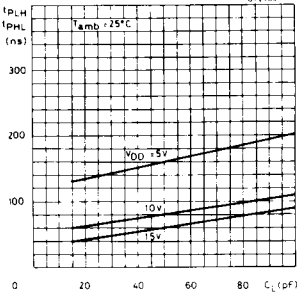
Minimum output high (source) current characteristics



Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance



Typical dynamic power dissipating vs. clock input frequency