LDO Voltage Regulator - Adjustable Output, Load Dump Protection

60 V, 100 mA

LM2931, NCV2931 Series

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input−to−output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power−up with mirror−image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor−based systems.

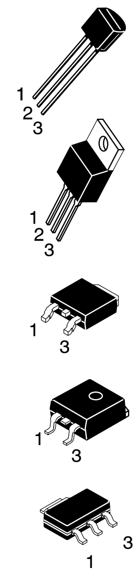
Features

- Input−to−Output Voltage Differential of < 0.6 V @ 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- −50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror−Image Protection
- Ideally Suited for Battery Powered Equipment
- Economical 5−Lead TO−220 Package with Two Optional Leadforms
- Available in Surface Mount SOP−8, D^{2}PAK and DPAK Packages
- High Accuracy (±2.5%) Reference (LM2931AC) Available
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- Pb−Free Packages are Available

Applications

- Battery Powered Consumer Products
- Hand−held Instruments
- Camcorders and Cameras

FIXED OUTPUT VOLTAGE



TO−92
Z SUFFIX
CASE 29−10

TO−220
T SUFFIX
CASE 221AB

Pin 1. Output
2. Ground
3. Input

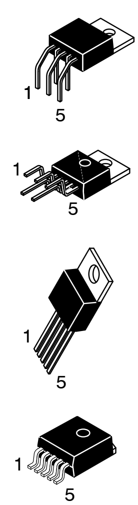
DPAK
DT SUFFIX
CASE 369C

D^{2}PAK
D2T SUFFIX
CASE 936

SOT−223
ST SUFFIX
CASE 318H

Pin 1. Input
2. Ground
3. Output

ADJUSTABLE OUTPUT VOLTAGE



TO−220
TH SUFFIX
CASE 314A

TO−220
TV SUFFIX
CASE 314B

TO−220
T SUFFIX
CASE 314D

D^{2}PAK
D2T SUFFIX
CASE 936A

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output

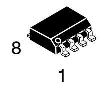
ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

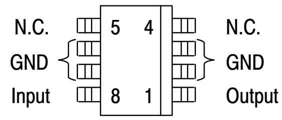
DEVICE MARKING INFORMATION

See general marking and heatsink information in the device marking section on page 14 of this data sheet.

SOIC−8
D SUFFIX
CASE 751

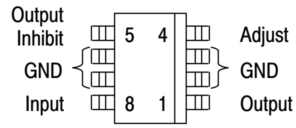


FIXED



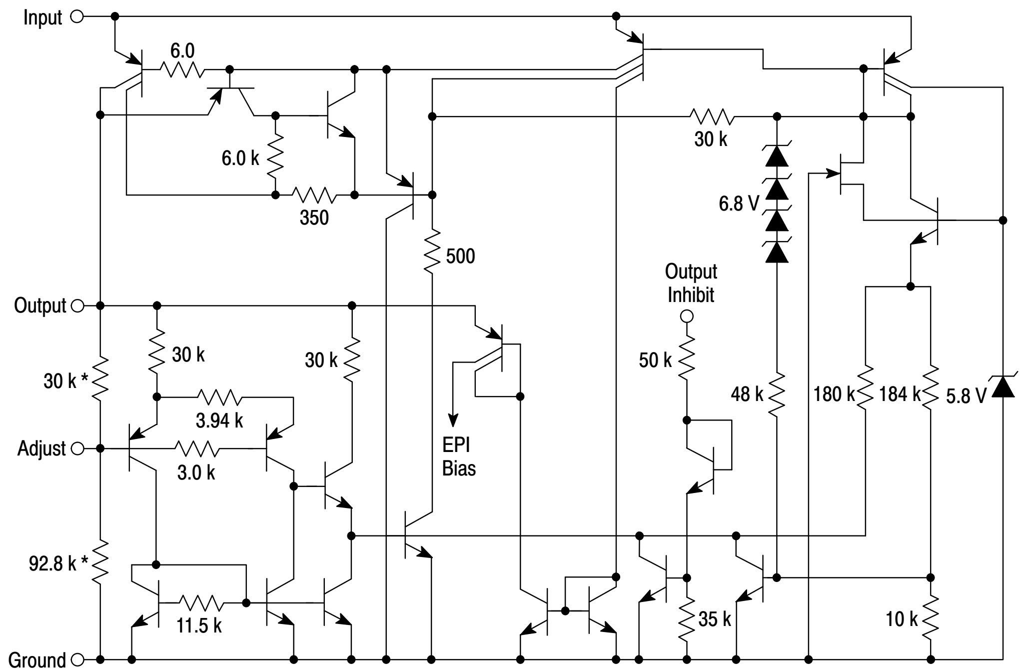
(Top View)

ADJUSTABLE



(Top View)

Representative Schematic Diagram



*Deleted on Adjustable Regulators

This device contains 26 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	40	Vdc
Transient Input Voltage ($\tau \leq$ 100 ms)	$V_I(\tau)$	60	Vpk
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq$ 100 ms	$-V_I(\tau)$	−50	Vpk
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Class 2, JESD22 A114−C Machine Model (MM) Class A, JESD22 A115−A Charged Device Model (CDM), JESD22 C101−C	 − − −	 2000 200 2000	 V V V
Power Dissipation Case 29 (TO−92 Type) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 221A, 314A, 314B and 314D (TO−220 Type) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 318H (SOT−223) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 369A (DPAK) (Note 1) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 751 (SOP−8) (Note 2) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 936 and 936A (D^2PAK) (Note 3) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 178 83 Internally Limited 65 5.0 Internally Limited 242 21 Internally Limited 92 6.0 Internally Limited 160 25 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W W °C/W °C/W W °C/W °C/W W °C/W °C/W W °C/W °C/W
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Operating Die Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. DPAK Junction−to−Ambient Thermal Resistance is for vertical mounting. Refer to Figure 25 for board mounted Thermal Resistance.
2. SOP−8 Junction−to−Ambient Thermal Resistance is for minimum recommended pad size. Refer to Figure 24 for Thermal Resistance variation versus pad size.
3. D^2PAK Junction−to−Ambient Thermal Resistance is for vertical mounting. Refer to Figure 26 for board mounted Thermal Resistance.
4. NCV rated devices are subjected to and meet the AECQ−100 quality standards.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_A = 25°C [Note 5])

Characteristic	Symbol	LM2931−5.0/NCV2931−5.0			LM2931A−5.0/NCV2931A−5.0			Unit
		Min	Typ	Max	Min	Typ	Max	
FIXED OUTPUT								
Output Voltage	V_O							V
V_{in} = 14 V, I_O = 10 mA, T_A = 25°C		4.75	5.0	5.25	4.81	5.0	5.19	
V_{in} = 6.0 V to 26 V, $I_O \le$ 100 mA, T_A = −40° to +125°C		4.50	–	5.50	4.75	–	5.25	
Line Regulation	Reg_{line}							mV
V_{in} = 9.0 V to 16 V		–	2.0	10	–	2.0	10	
V_{in} = 6.0 V to 26 V		–	4.0	30	–	4.0	30	
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	14	50	–	14	50	mV
Output Impedance	Z_O							mΩ
I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz		–	200	–	–	200	–	
Bias Current	I_B							mA
V_{in} = 14 V, I_O = 100 mA, T_A = 25°C		–	5.8	30	–	5.8	30	
V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_A = −40° to +125°C		–	0.4	1.0	–	0.4	1.0	
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	700	–	–	700	–	μVrms
Long Term Stability	S	–	20	–	–	20	–	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	–	60	90	–	dB
Dropout Voltage	V_I−V_O							V
I_O = 10 mA		–	0.015	0.2	–	0.015	0.2	
I_O = 100 mA		–	0.16	0.6	–	0.16	0.6	
Over−Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	–	−0.3	0	–	V

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. NCV devices are qualified for automotive use.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_A = 25°C [Note 7])

Characteristic	Symbol	LM2931C/NCV2931C			LM2931AC/NCV2931AC			Unit
		Min	Typ	Max	Min	Typ	Max	
ADJUSTABLE OUTPUT								
Reference Voltage (Note 8, Figure 18) I_O = 10 mA, T_A = 25°C $I_O \leq$ 100 mA, T_A = −40 to +125°C	V_{ref}	 1.14 1.08	 1.20 –	 1.26 1.32	 1.17 1.15	 1.20 –	 1.23 1.25	V
Output Voltage Range	$V_{O\ range}$	3.0 to 24	2.7 to 29.5	–	3.0 to 24	2.7 to 29.5	–	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}	–	0.2	1.5	–	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	0.3	1.0	–	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	 –	 40	 –	 –	 40	 –	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 – – –	 6.0 0.4 0.2	 – 1.0 1.0	 – – –	 6.0 0.4 0.2	 – 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	–	0.2	–	–	0.2	–	μA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	140	–	–	140	–	μVrms/V
Long−Term Stability	S	–	0.4	–	–	0.4	–	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	–	0.10	0.003	–	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_I−V_O	 – –	 0.015 0.16	 0.2 0.6	 – –	 0.015 0.16	 0.2 0.6	V
Over−Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	–	−0.3	0	–	V
Output Inhibit Threshold Voltages Output “On”: T_A = 25°C T_A = −40° to +125°C Output “Off”: T_A = 25°C T_A = −40° to +125°C	$V_{th(OI)}$	 – – 2.50 3.25	 2.15 – 2.26 –	 1.90 1.20 – –	 – – 2.50 3.25	 2.15 – 2.26 –	 1.90 1.20 – –	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	–	30	50	–	30	50	μA

7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
8. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

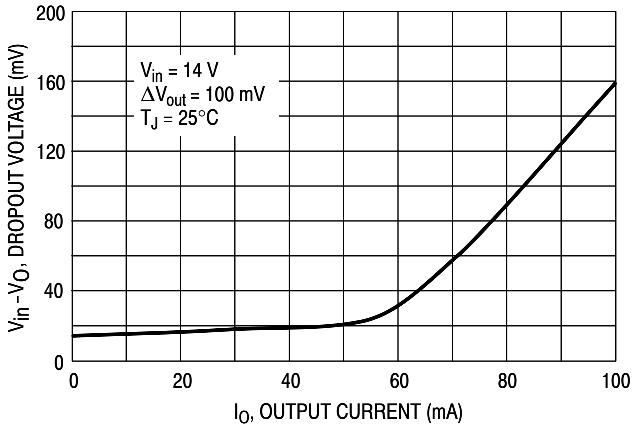


Figure 1. Dropout Voltage versus Output Current

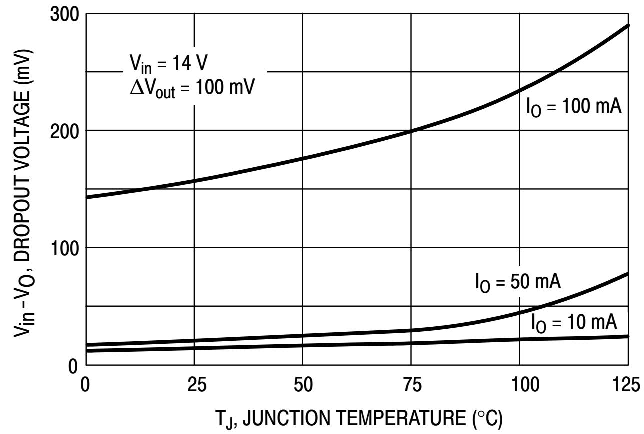


Figure 2. Dropout Voltage versus Junction Temperature

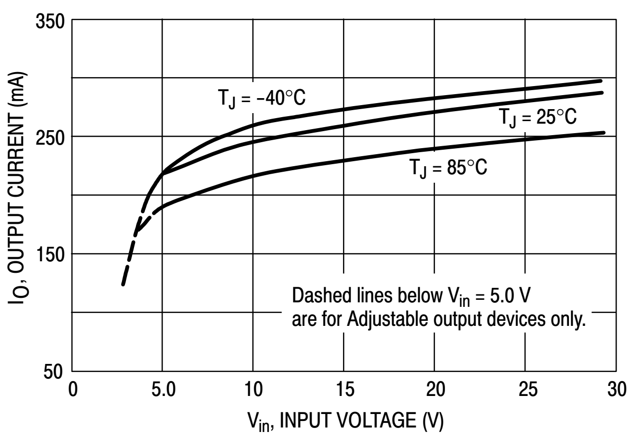


Figure 3. Peak Output Current versus Input Voltage

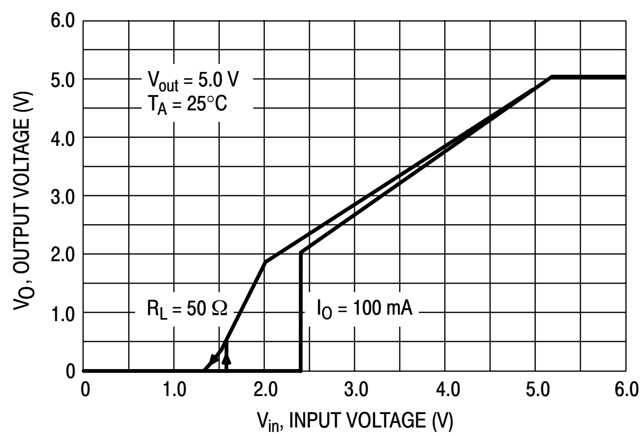


Figure 4. Output Voltage versus Input Voltage

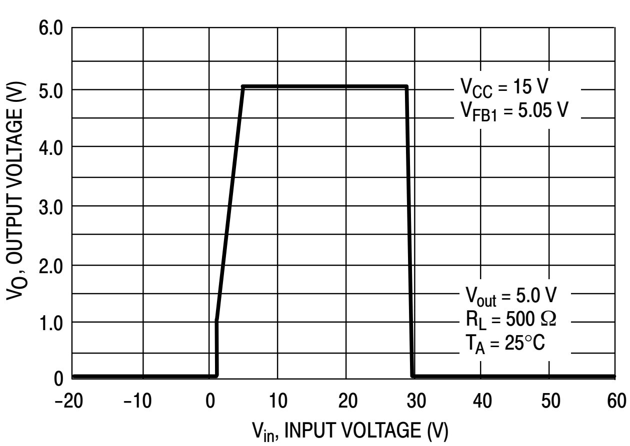


Figure 5. Output Voltage versus Input Voltage

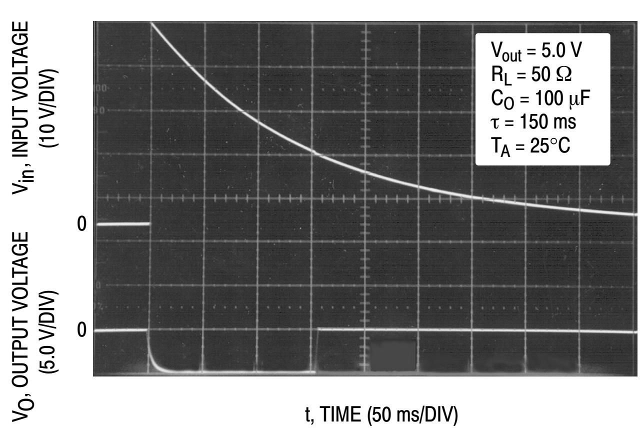


Figure 6. Load Dump Characteristics

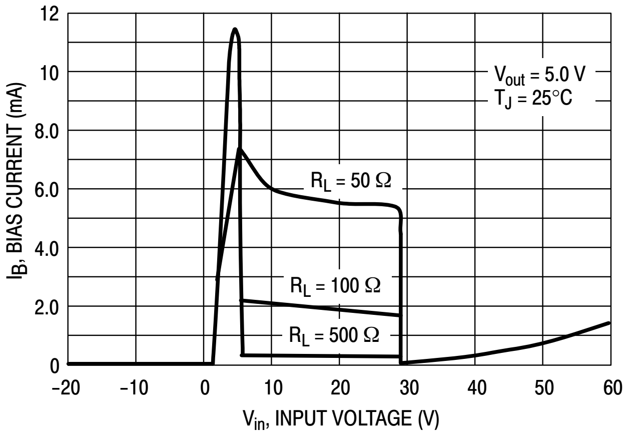


Figure 7. Bias Current versus Input Voltage

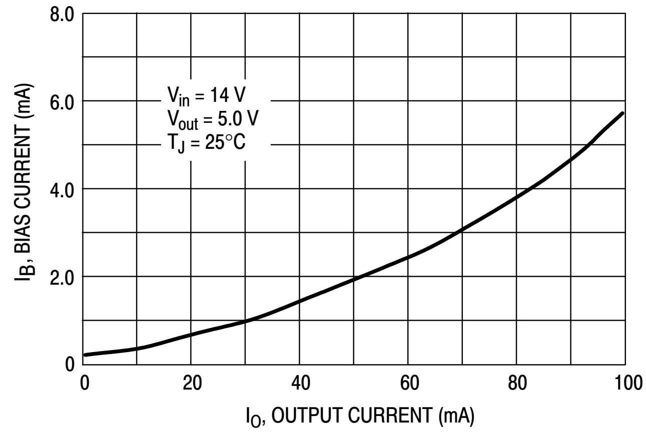


Figure 8. Bias Current versus Output Current

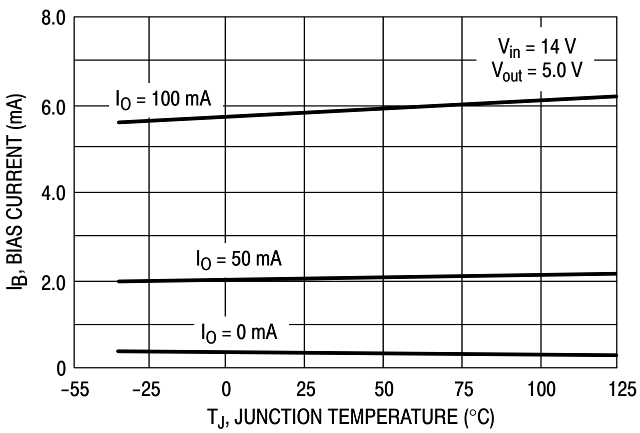


Figure 9. Bias Current versus Junction Temperature

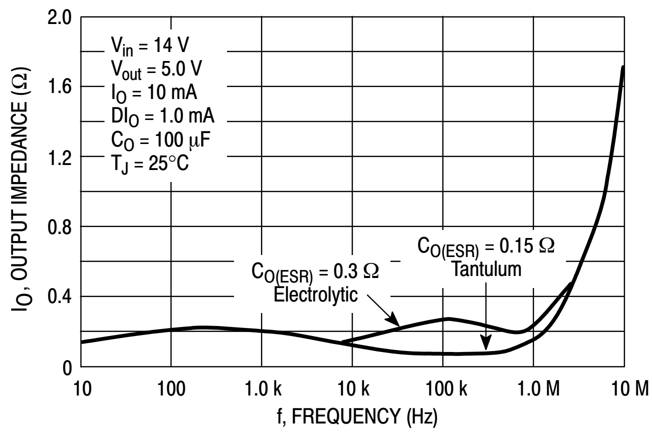


Figure 10. Output Impedance versus Frequency

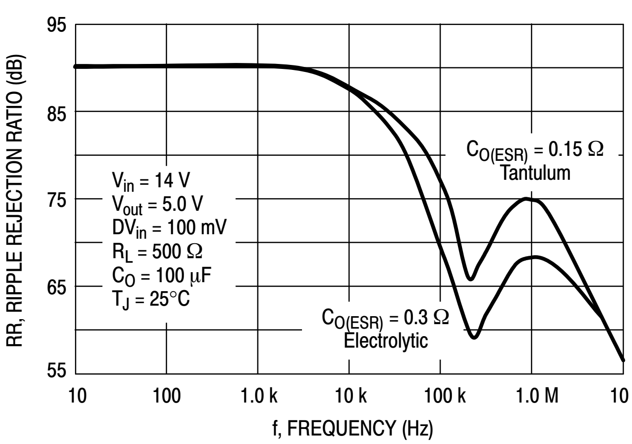


Figure 11. Ripple Rejection versus Frequency

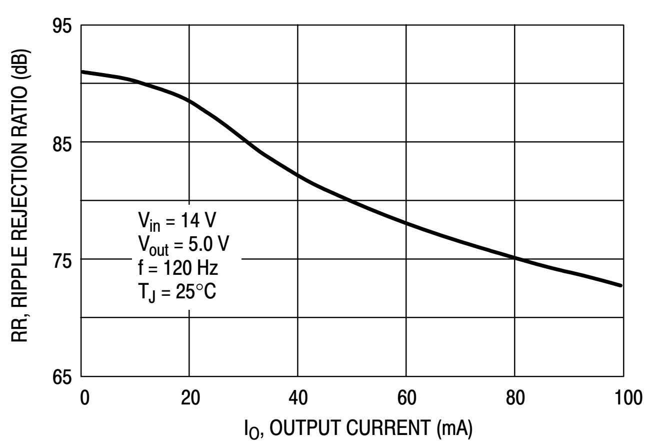


Figure 12. Ripple Rejection versus Output Current

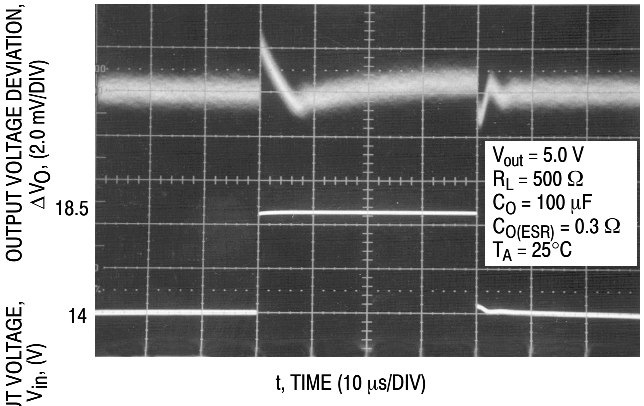


Figure 13. Line Regulation

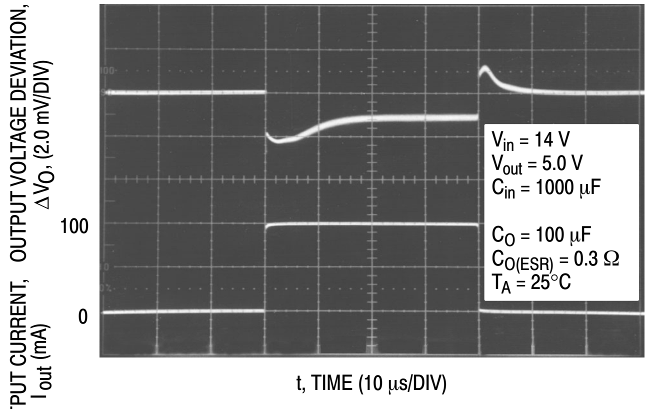


Figure 14. Load Regulation

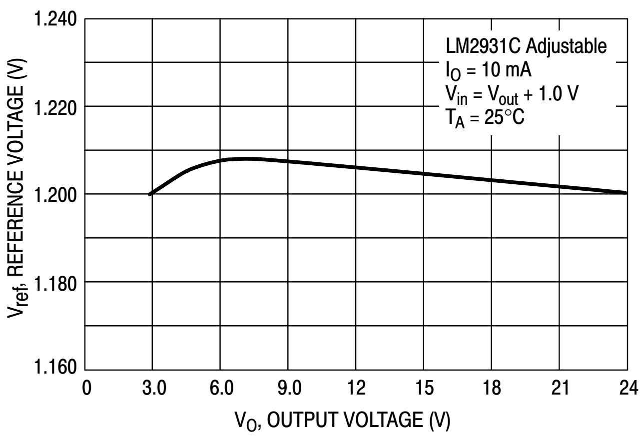


Figure 15. Reference Voltage versus Output Voltage

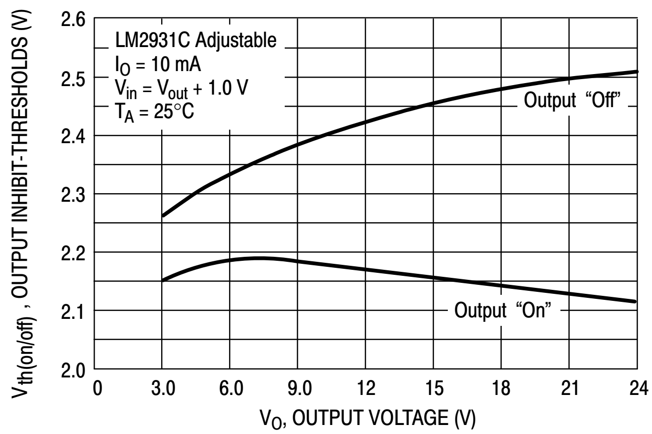


Figure 16. Output Inhibit−Thresholds versus Output Voltage

APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow−out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power−up with mirror−image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around −30°C, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of −40° to +85°C and −55° to +105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll−off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under−damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable". It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

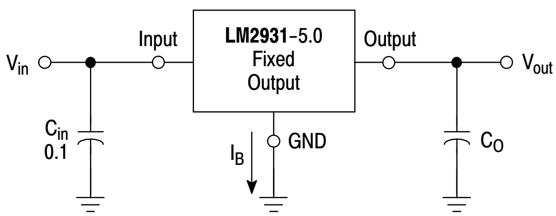
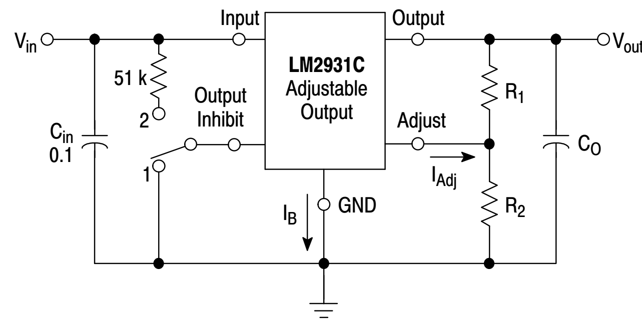


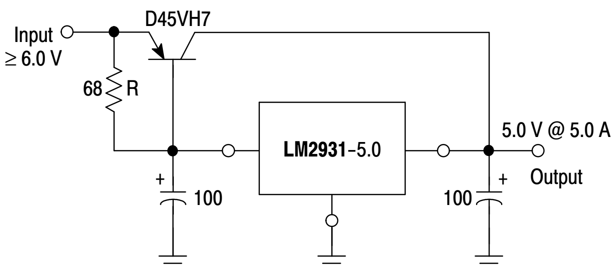
Figure 17. Fixed Output Regulator



Switch Position 1 = Output “On”, 2 = Output “Off”

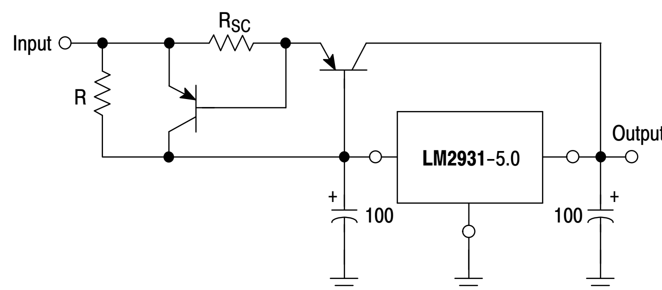
$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2 \qquad 22.5\ k \geq \frac{R_1 R_2}{R_1 + R_2}$$

Figure 18. Adjustable Output Regulator



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short circuit proof.

Figure 19. (5.0 A) Low Differential Voltage Regulator



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

Figure 20. Current Boost Regulator with Short Circuit Projection

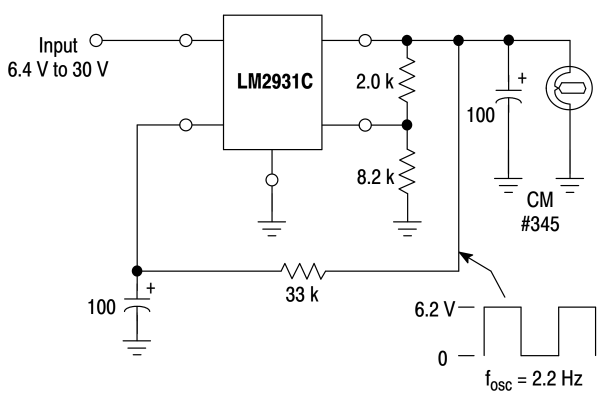


Figure 21. Constant Intensity Lamp Flasher

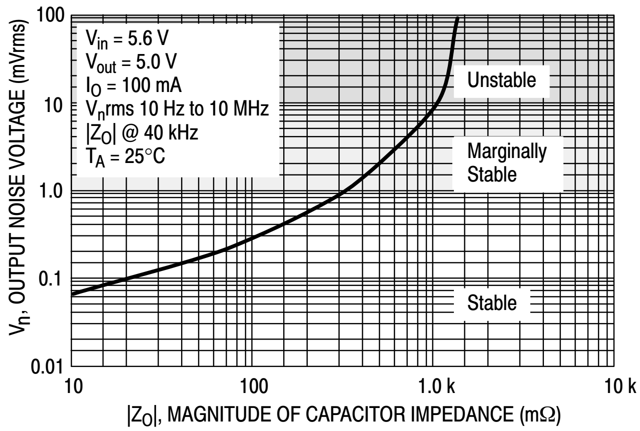


Figure 22. Output Noise Voltage vs. Output Capacitor Impedance

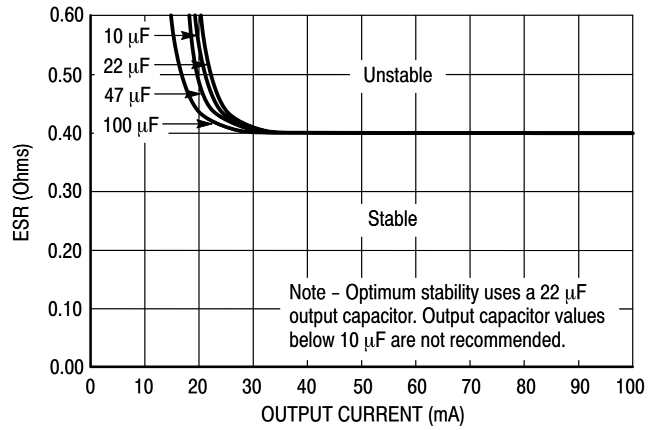


Figure 23. Output Capacitor ESR Stability vs. Output Load Current

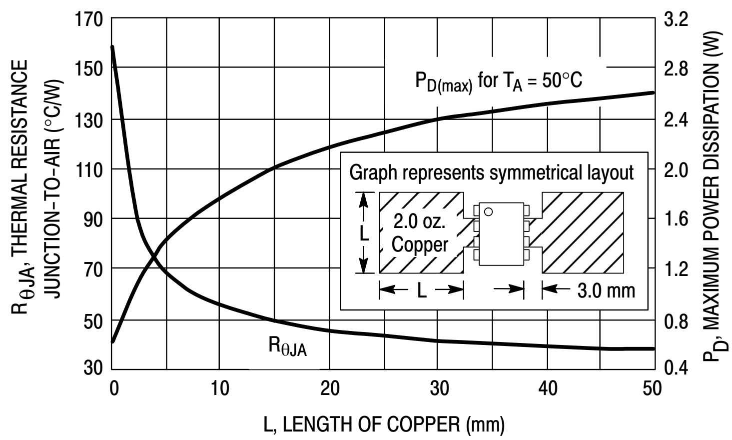


Figure 24. SOP−8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

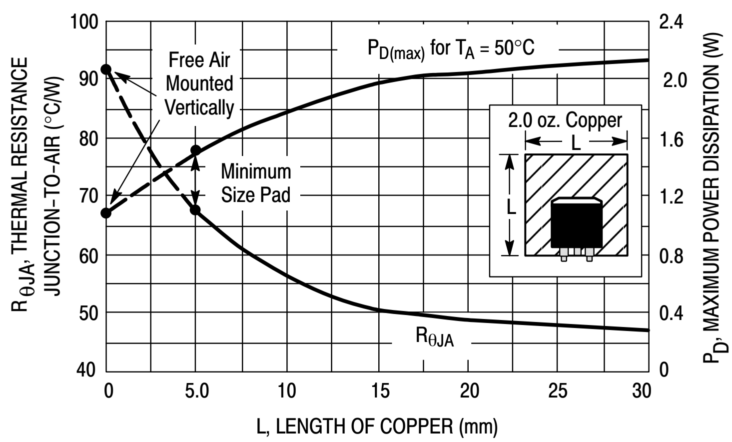


Figure 25. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

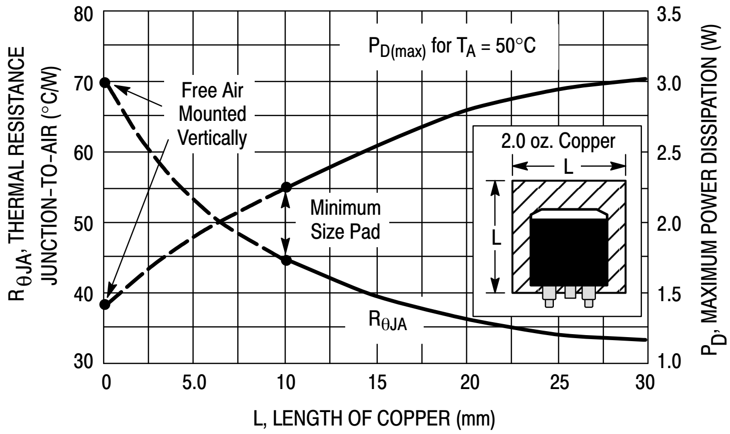


Figure 26. 3−Pin and 5−Pin D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

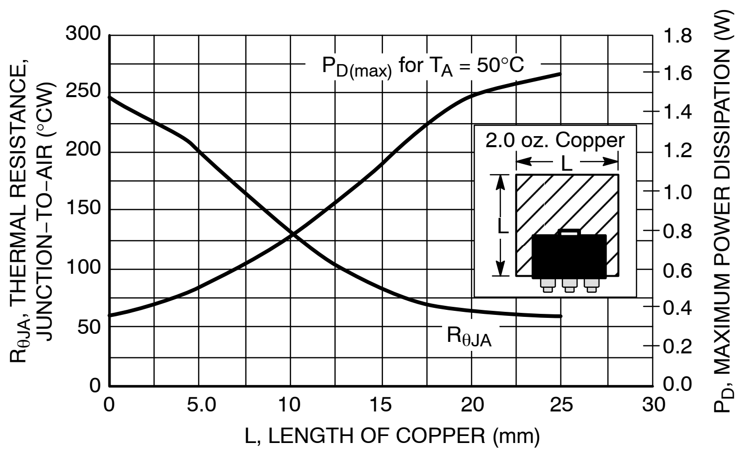


Figure 27. SOT−223 Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length

DEFINITIONS

Dropout Voltage − The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation − The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation − The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation − The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current − That part of the input current that is not delivered to the load.

Output Noise Voltage − The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long−Term Stability − Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

ORDERING INFORMATION

Device	Output		Package	Shipping†
	Voltage	Tolerance		
LM2931AD−5.0G	5.0 V	±3.8%	SOIC−8 (Pb−Free)	98 Units / Rail
LM2931AD−5.0R2G	5.0 V	±3.8%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2931ADT−5.0RKG	5.0 V	±3.8%	DPAK (Pb−Free)	2500 / VacPk
LM2931AD2T−5R4G	5.0 V	±3.8%	D^2PAK (Pb−Free)	800 / VacPk Reel
LM2931AT−5.0G	5.0 V	±3.8%	TO−220 (Pb−Free)	50 Units / Rail
LM2931AZ−5.0G	5.0 V	±3.8%	TO−92 (Pb−Free)	2000 / Inner Bag
LM2931AZ−5.0RAG	5.0 V	±3.8%	TO−92 (Pb−Free)	2000 / Tape & Reel
LM2931AZ−5.0RPG	5.0 V	±3.8%	TO−92 (Pb−Free)	2000 / Ammo Pack
LM2931D−5.0R2G	5.0 V	±5.0%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2931D2T−5.0R4G	5.0 V	±5.0%	D^2PAK (Pb−Free)	800 / VacPk Reel
LM2931DT−5.0G	5.0 V	±5.0%	DPAK (Pb−Free)	75 Units / Rail
LM2931T−5.0G	5.0 V	±5.0%	TO−220 (Pb−Free)	50 Units / Rail
LM2931Z−5.0G	5.0 V	±5.0%	TO−92 (Pb−Free)	2000 / Inner Bag
LM2931Z−5.0RAG	5.0 V	±5.0%	TO−92 (Pb−Free)	2000 / Tape & Reel
LM2931Z−5.0RPG	5.0 V	±5.0%	TO−92 (Pb−Free)	2000 / Ammo Pack
LM2931CDG	Adjustable	±5.0%	SOIC−8 (Pb−Free)	98 Units / Rail
LM2931CDR2G	Adjustable	±5.0%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2931ACDR2G	Adjustable	±2.0%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2931ACD2TR4G	Adjustable	±2.0%	D^2PAK (Pb−Free)	800 / VacPk Reel
NCV2931ACDR2G*	Adjustable	±2.5%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2931AD−5.0R2G*	5.0 V	±3.8%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2931AST−5.0T3G*	5.0 V	±3.8%	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV2931AZ−5.0G*	5.0 V	±3.8%	TO−92 (Pb−Free)	2000 / Inner Bag

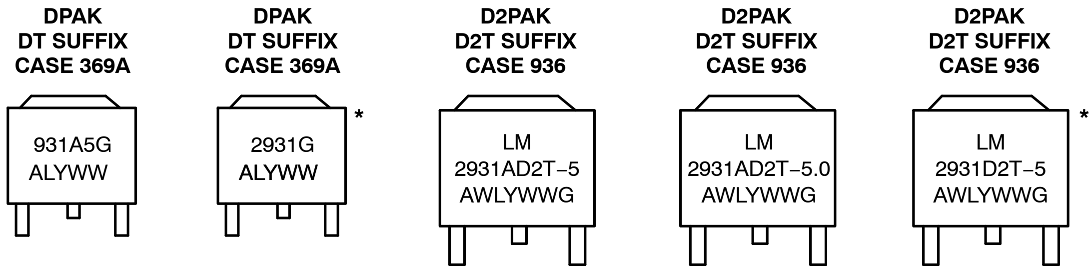
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV2931: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ORDERING INFORMATION (continued)

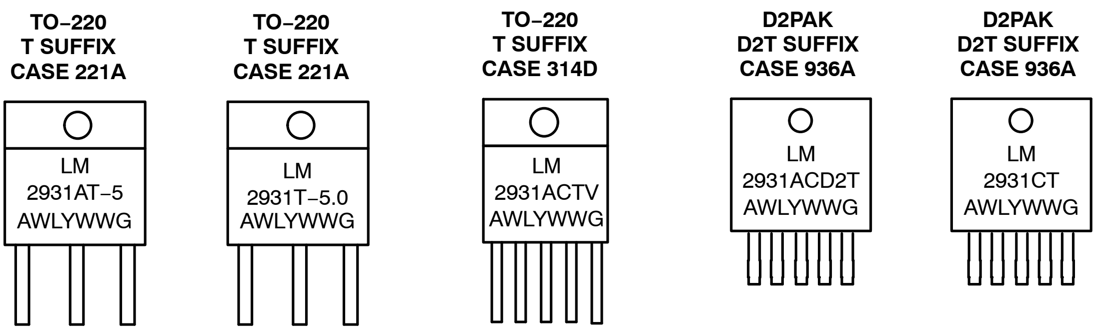
Device	Output		Package	Shipping†
	Voltage	Tolerance		
NCV2931AZ−5.0RAG*	5.0 V	±3.8%	TO−92 (Pb−Free)	2000 / Tape & Reel
NCV2931CDR2G*	Adjustable	±5.0%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2931D−5.0R2G*	5.0 V	±5.0%	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2931ADT5.0RKG*	5.0 V	±3.8%	DPAK (Pb−Free)	2500 / Tape & Reel
NCV2931DT−5.0RKG*	5.0 V	±5.0%	DPAK (Pb−Free)	2500 / Tape & Reel
NCV2931ACD2TR4G*	Adjustable	±2.5%	D^2PAK (Pb−Free)	800 / VacPk Reel
NCV2931D2T5.0R4G*	5.0 V	±5.0%	D^2PAK (Pb−Free)	800 / VacPk Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV2931: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS



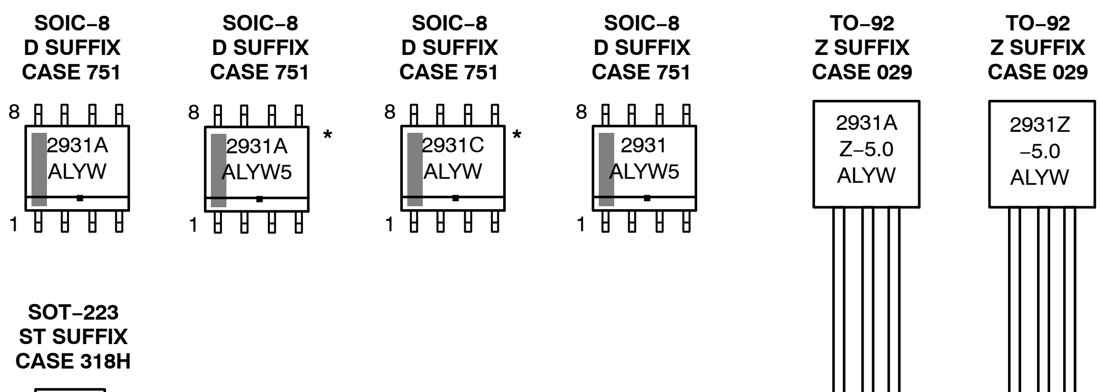
Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

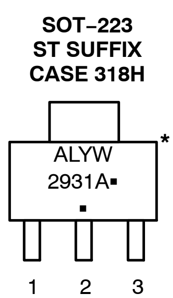


Heatsink surface connected to Pin 2.

Heatsink surface connected to Pin 3.

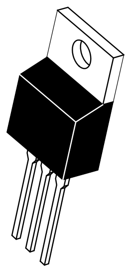
Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.





A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Device

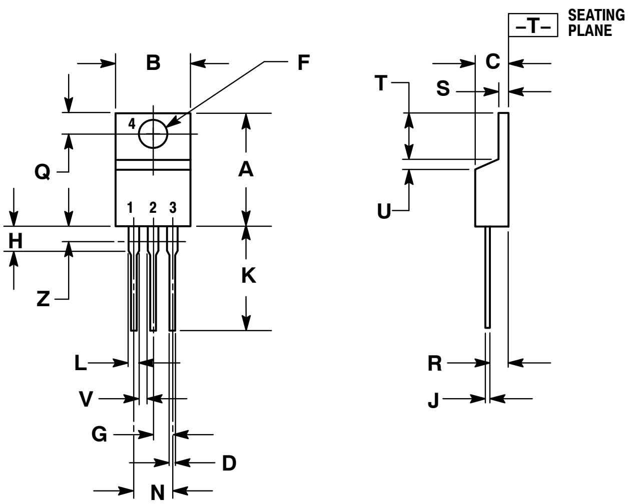
*This marking diagram also applies to NCV2931.



SCALE 1:1

TO−220, SINGLE GAUGE
CASE 221AB−01
ISSUE A

DATE 16 NOV 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS S = 0.045 − 0.055 INCHES (1.143 − 1.397 MM)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.024	0.508	0.61
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

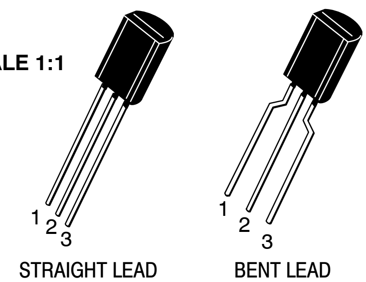
STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

DOCUMENT NUMBER:	98AON23085D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−220, SINGLE GAUGE	PAGE 1 OF 1

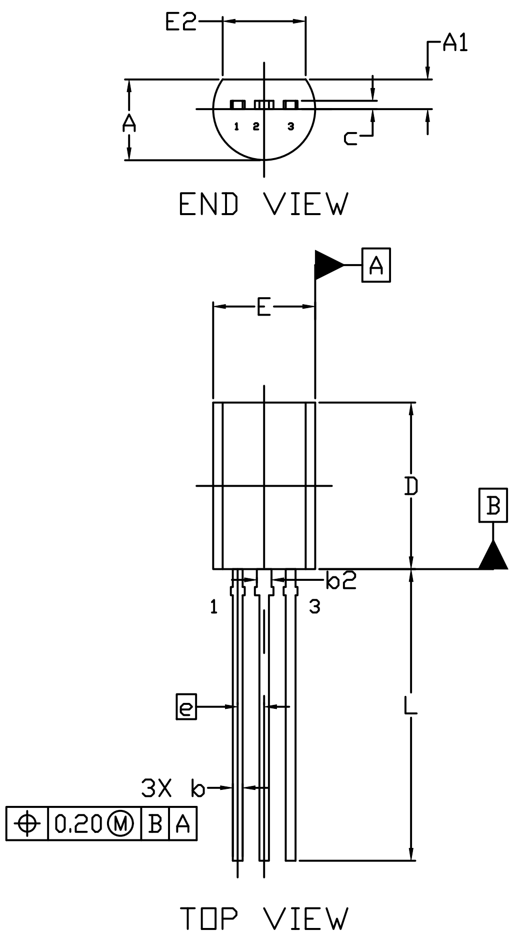
SCALE 1:1



TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

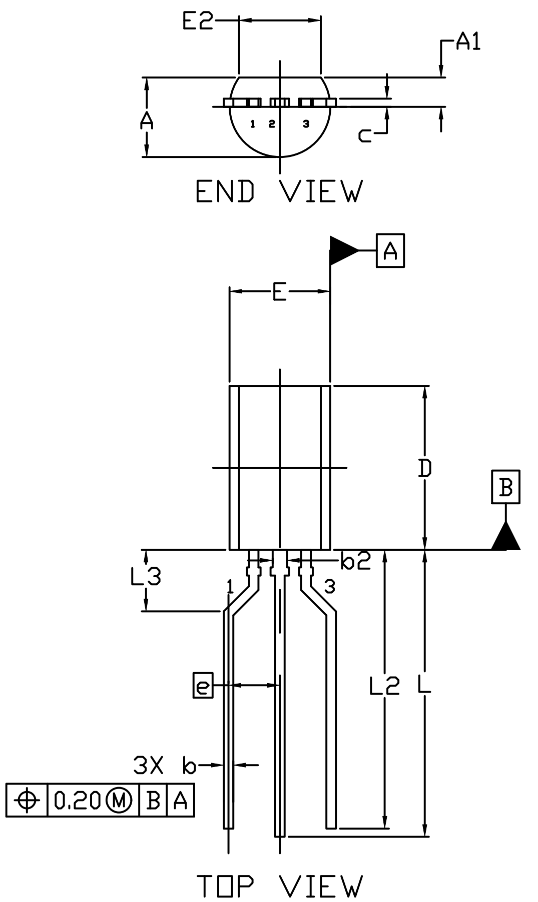
STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 2 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC
MARKING DIAGRAM*

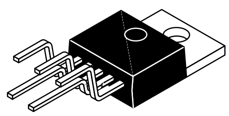
XXXXX
XXXXX
ALYW▪
▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

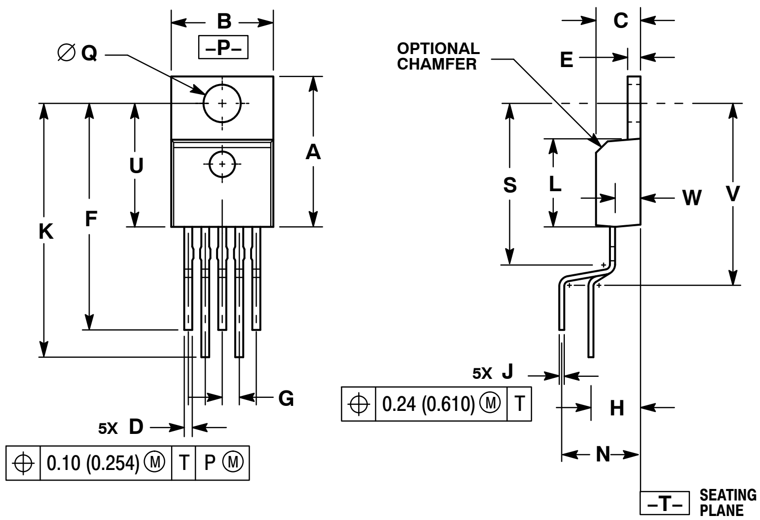
DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−92 (TO−226) 1 WATT	PAGE 3 OF 3



SCALE 1:1

TO−220 5 LEAD OFFSET
CASE 314B−05
ISSUE L

DATE 01/07/1994



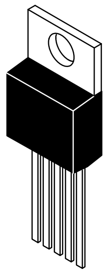
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	---	0.620	---	15.748
U	0.468	0.505	11.888	12.827
V	---	0.735	---	18.669
W	0.090	0.110	2.286	2.794

STYLE 1 THRU 4:
CANCELLED

STYLE 5:
PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

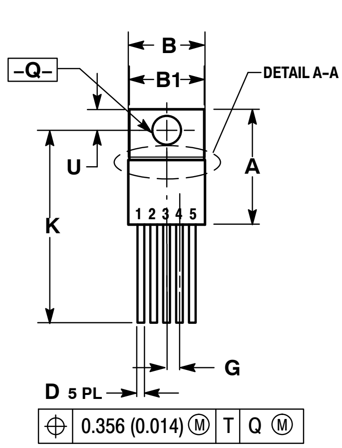
DOCUMENT NUMBER:	98ASB42218B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO−220 5 LEAD OFFSET	PAGE 1 OF 1

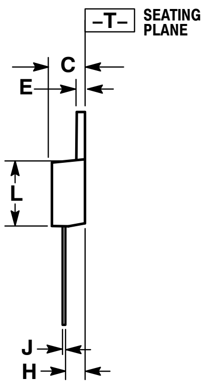


SCALE 1:1

TO−220 5−LEAD
CASE 314D−04
ISSUE H

DATE 29 JAN 2010

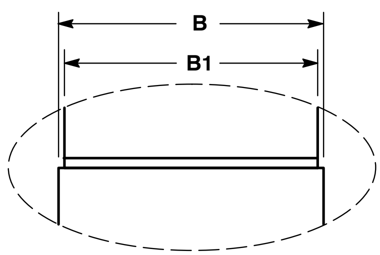




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

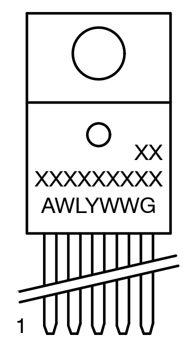
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
B1	0.375	0.415	9.525	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.977	1.045	24.810	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

STYLE 1 THRU 4:
1. OBSOLETE



DETAIL A−A

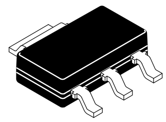
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

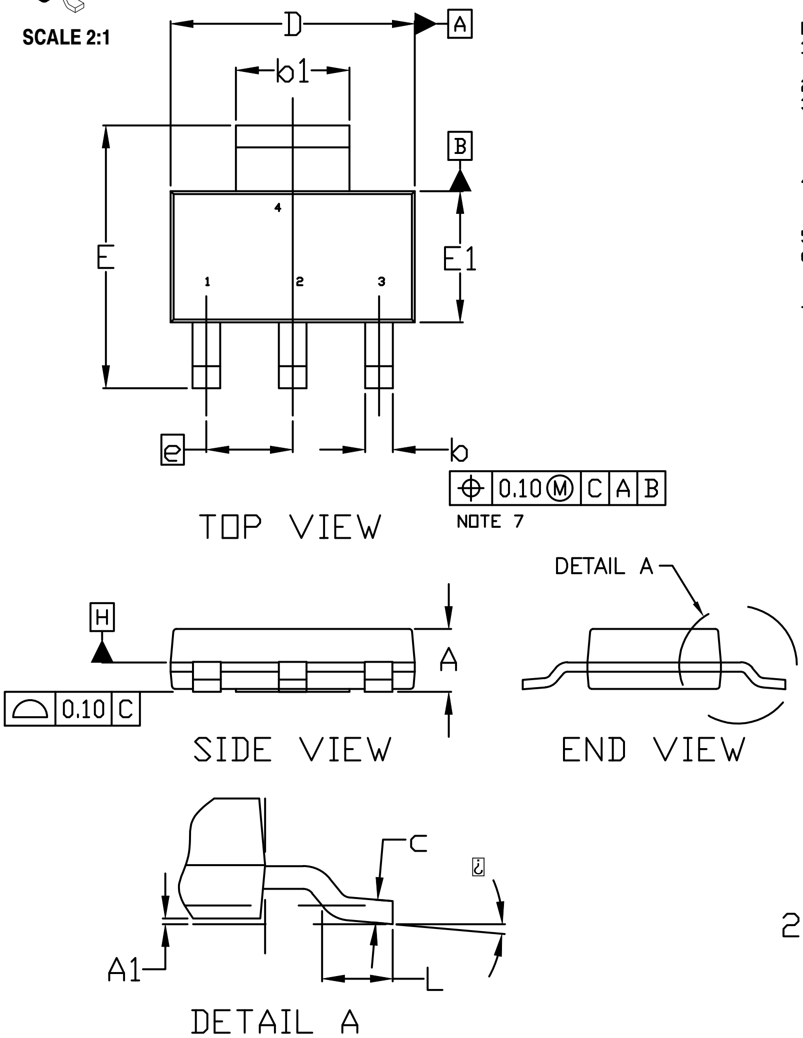
DOCUMENT NUMBER:	**98ASB42220B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−220 5−LEAD**	**PAGE 1 OF 1**



SCALE 2:1

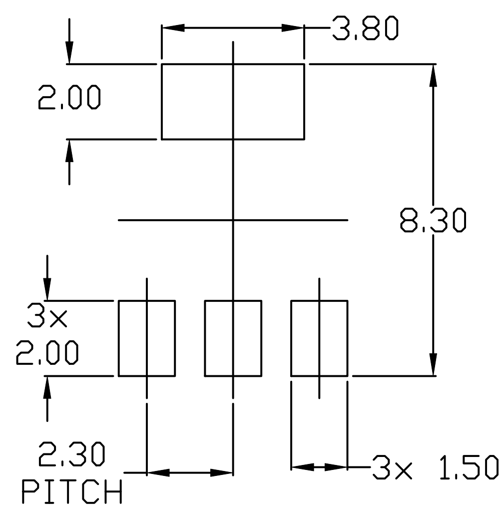
SOT−223
CASE 318H
ISSUE B

DATE 13 MAY 2020



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

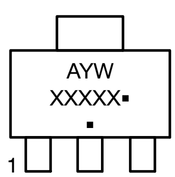
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
¿	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

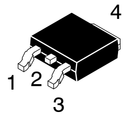


A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

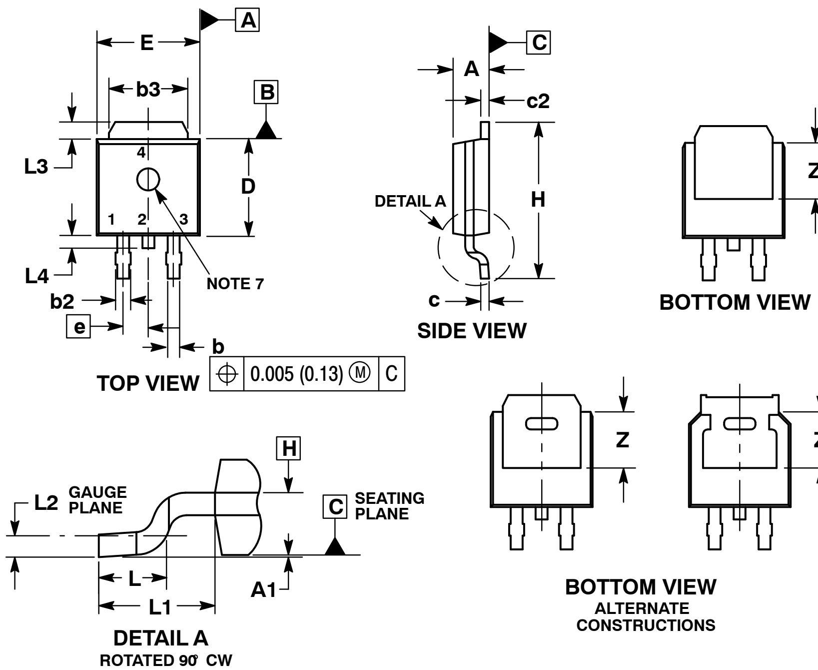
DOCUMENT NUMBER:	**98ASH70634A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−223**	**PAGE 1 OF 1**



SCALE 1:1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

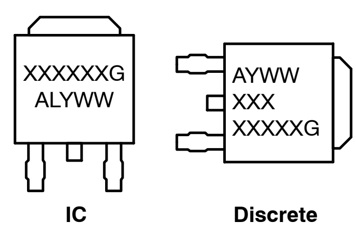
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

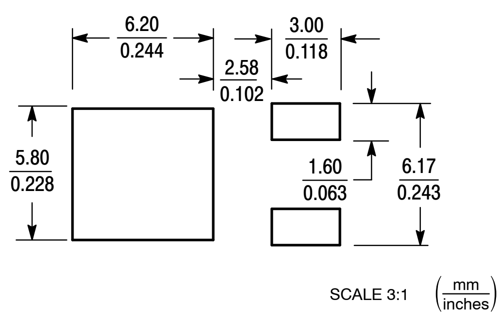
GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

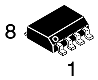
*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

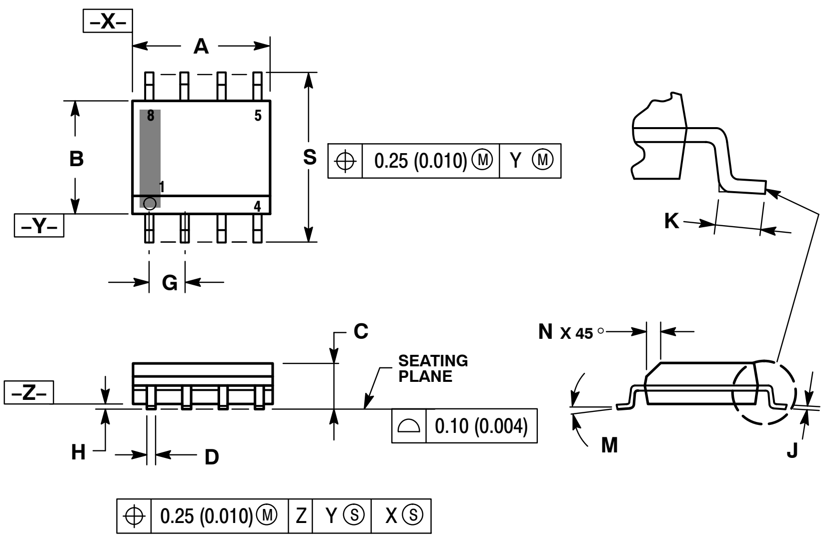
DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

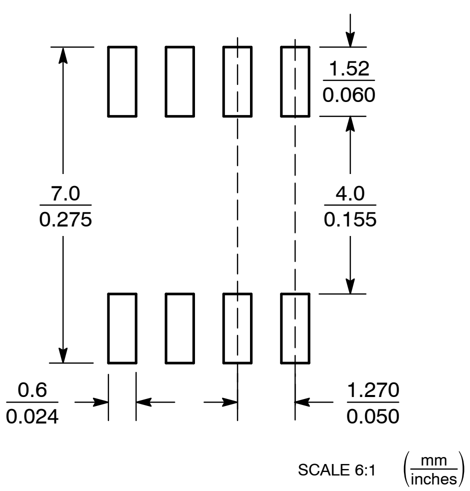
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

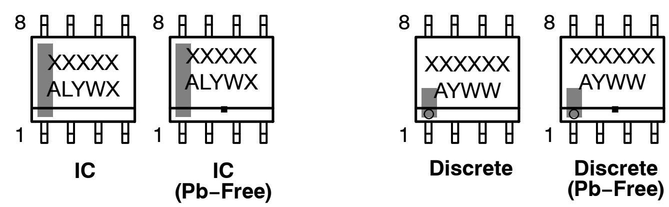
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

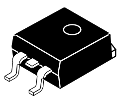
STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

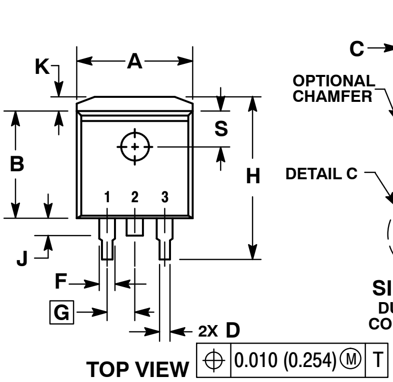
STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1



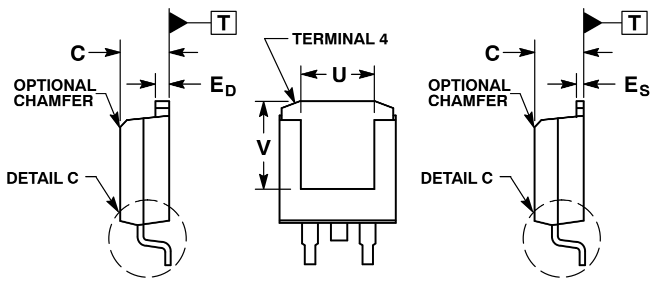
SCALE 1:1

D²PAK
CASE 936−03
ISSUE E

DATE 29 SEP 2015



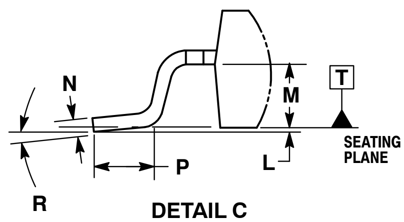
TOP VIEW



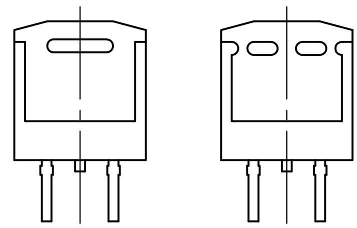
SIDE VIEW DUAL GAUGE CONSTRUCTION

BOTTOM VIEW

SIDE VIEW SINGLE GAUGE CONSTRUCTION



DETAIL C

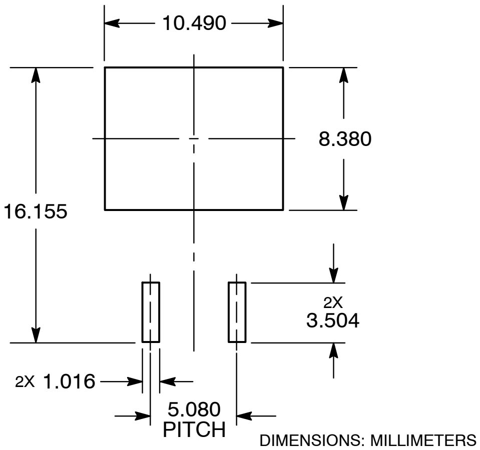


BOTTOM VIEW OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

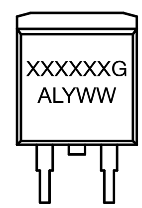
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E_D	0.045	0.055	1.143	1.397
E_S	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

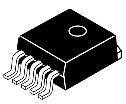
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

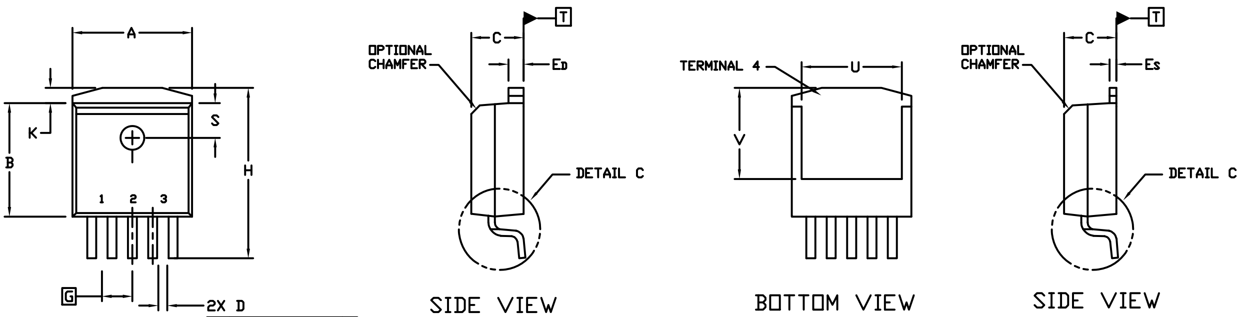
DOCUMENT NUMBER:	98ASH01005A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	D²PAK	PAGE 1 OF 1



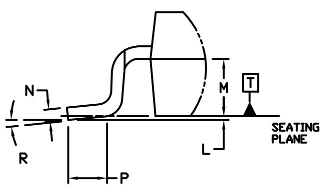
SCALE 1:1

D²PAK 5−LEAD
CASE 936A−02
ISSUE E

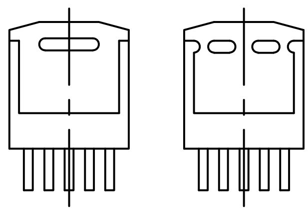
DATE 28 JUL 2021



TOP VIEW — SIDE VIEW (DUAL GUAGE CONSTRUCTION) — BOTTOM VIEW — SIDE VIEW (SINGLE GUAGE CONSTRUCTION)



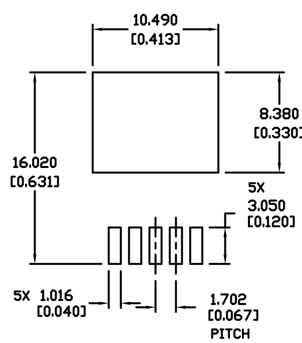
DETAIL C
TIP LEADFORM
ROTATED 90° CW



BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

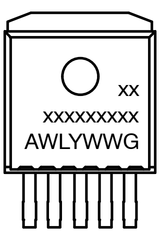
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



xxxxxx	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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