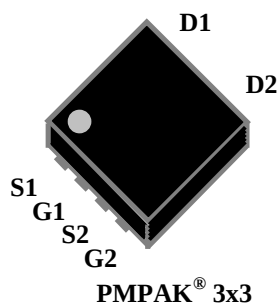


- ▼ Simple Drive Requirement
- ▼ Good Thermal Performance
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

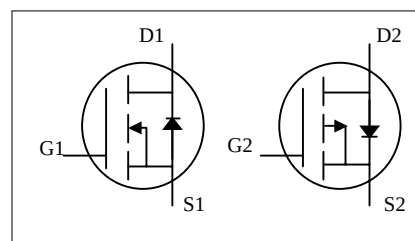


Description

XP3700 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 3x3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	20m Ω
	I_D^3	8.7A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	45m Ω
	I_D^3	-6.1A



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	+20	+20	V
$I_D@T_A=25^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	8.7	-6.1	A
$I_D@T_A=70^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	6.9	-4.9	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2.5		W
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	8	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	50	°C/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =8A	-	-	20	mΩ
		V _{GS} =4.5V, I _D =4A	-	-	35	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =1mA	1.4	-	2.5	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =8A	-	23	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =4A	-	5	8	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	1.8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	1.8	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	7	-	ns
t _r	Rise Time	I _D =1A	-	10	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω	-	19	-	ns
t _f	Fall Time	V _{GS} =10V	-	4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	550	880	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	90	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =2A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =8A, V _{GS} =0V	-	10	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-6A	-	-	45	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	85	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-2.5	V
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-6A	-	9	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V	-	-	-10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =-3A V _{DS} =-15V V _{GS} =-4.5V	-	6	9.6	nC
Q _{gs}	Gate-Source Charge		-	1.8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge		-	2.1	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =-15V I _D =-1A R _G =6Ω	-	10	-	ns
t _r	Rise Time		-	11	-	ns
t _{d(off)}	Turn-off Delay Time		-	30	-	ns
t _f	Fall Time	V _{GS} =-10V	-	14	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V V _{DS} =-15V f=1.0MHz	-	610	976	pF
C _{oss}	Output Capacitance		-	100	-	pF
C _{rss}	Reverse Transfer Capacitance		-	70	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{SD}	Forward On Voltage ²	I _S =-2A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	I _S =-6A, V _{GS} =0V dI/dt=-100A/μs	-	12	-	ns
Q _{rr}	Reverse Recovery Charge		-	4	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec, 90°C/W at steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

N-Channel

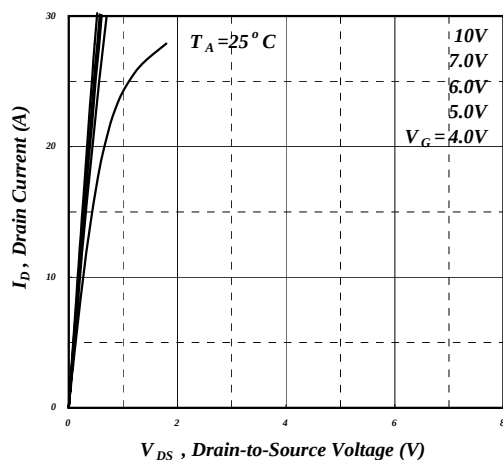


Fig 1. Typical Output Characteristics

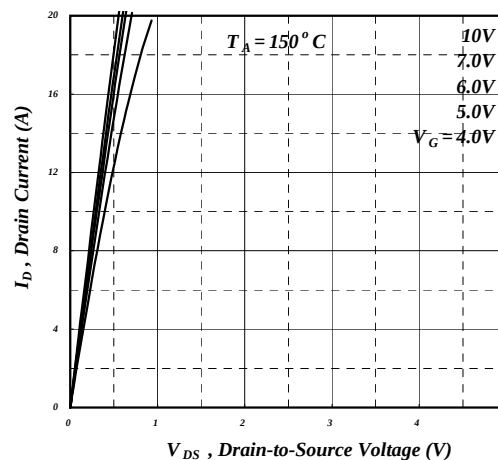


Fig 2. Typical Output Characteristics

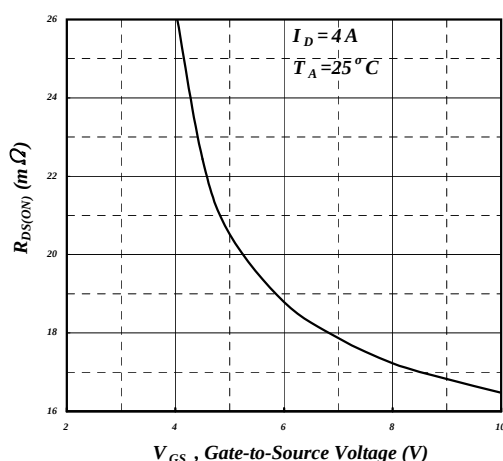


Fig 3. On-Resistance v.s. Gate Voltage

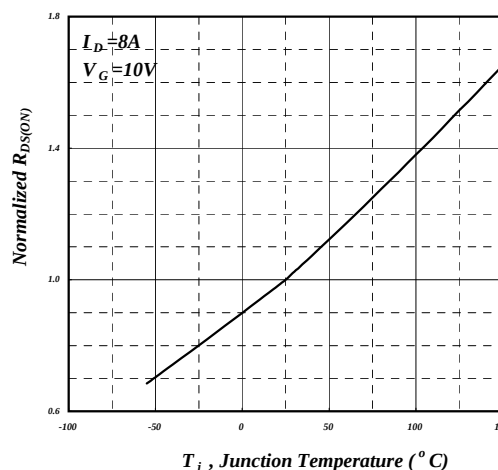


Fig 4. Normalized On-Resistance v.s. Junction Temperature

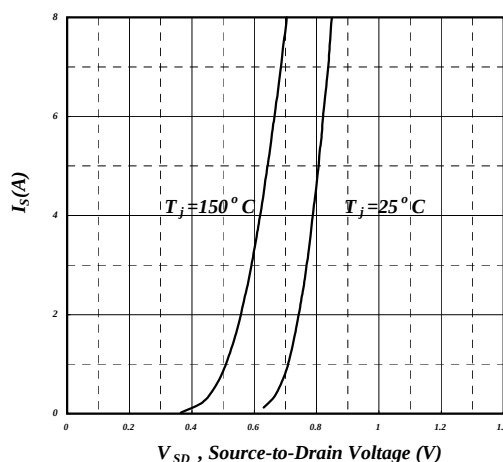


Fig 5. Forward Characteristic of Reverse Diode

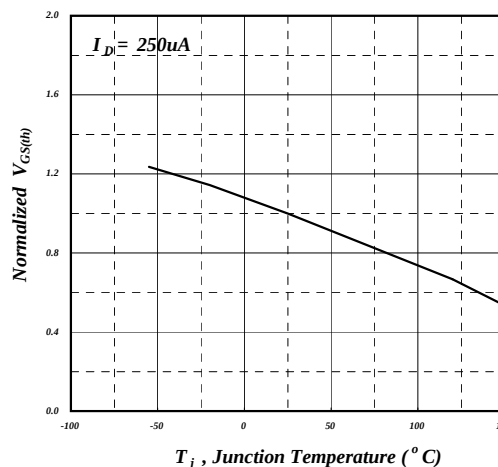


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

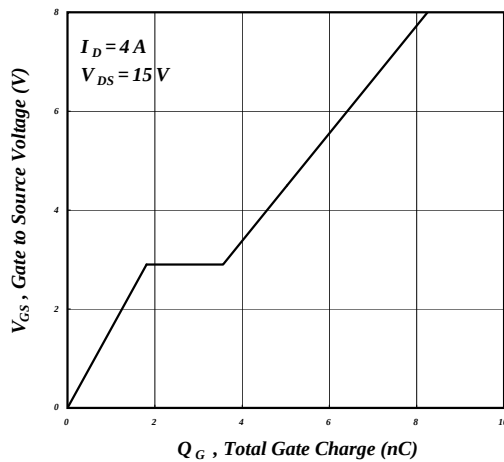


Fig 7. Gate Charge Characteristics

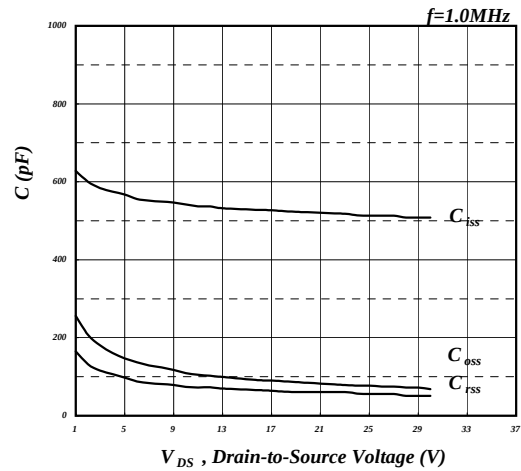


Fig 8. Typical Capacitance Characteristics

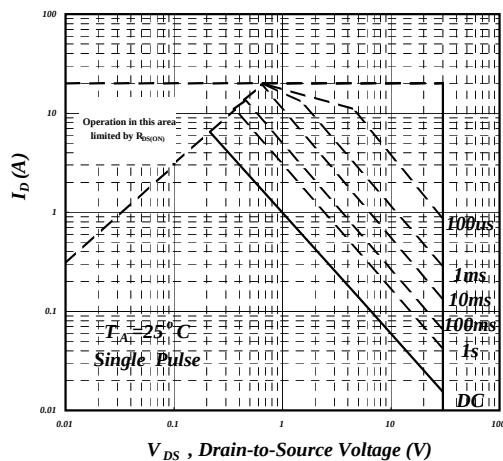


Fig 9. Maximum Safe Operating Area

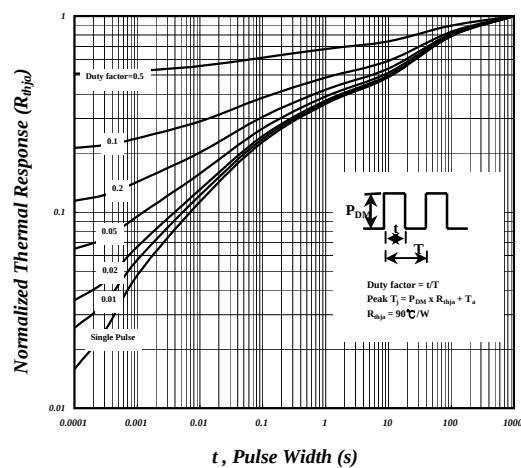


Fig 10. Effective Transient Thermal Impedance

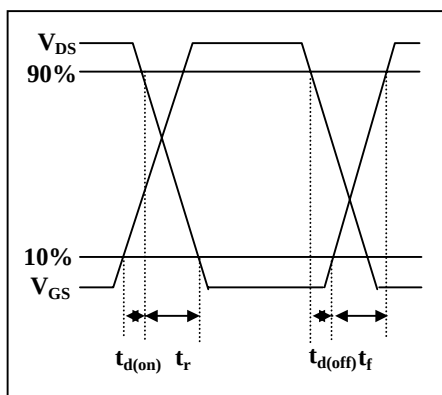


Fig 11. Switching Time Waveform

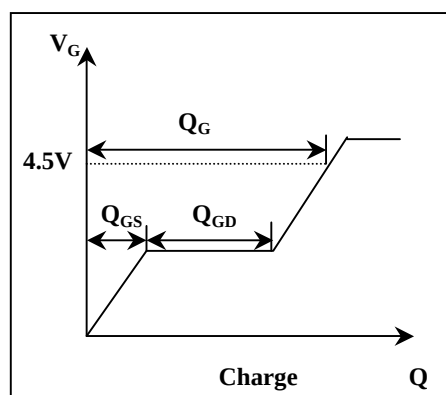


Fig 12. Gate Charge Waveform

P-Channel

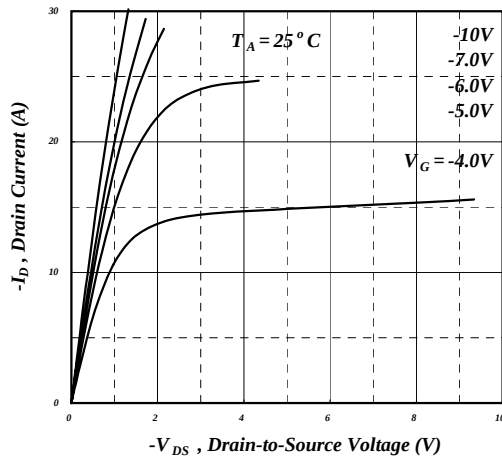


Fig 1. Typical Output Characteristics

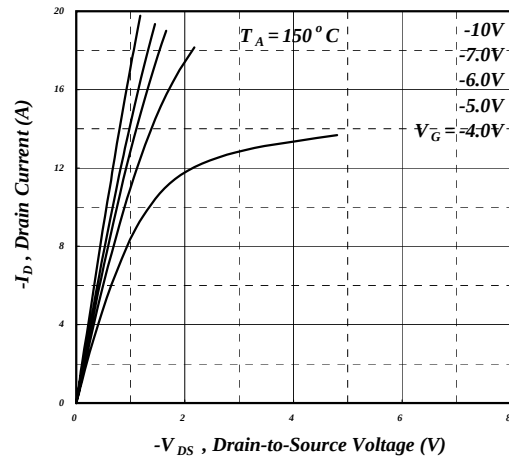


Fig 2. Typical Output Characteristics

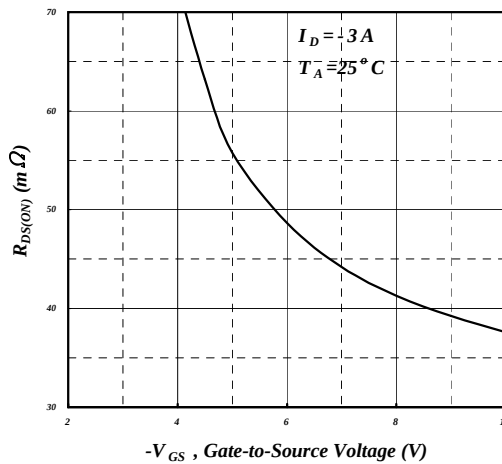
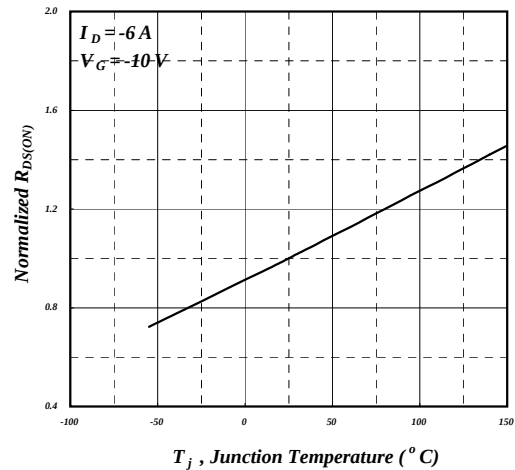
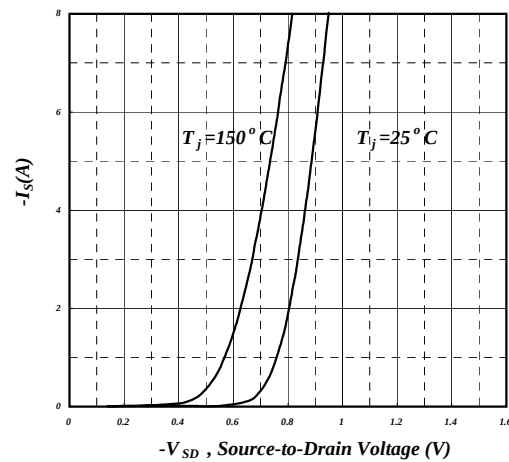


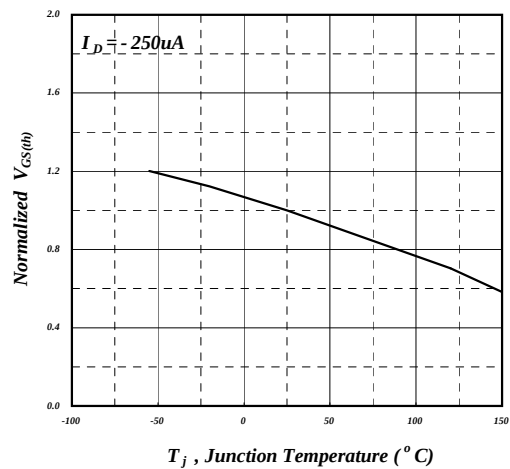
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

P-Channel

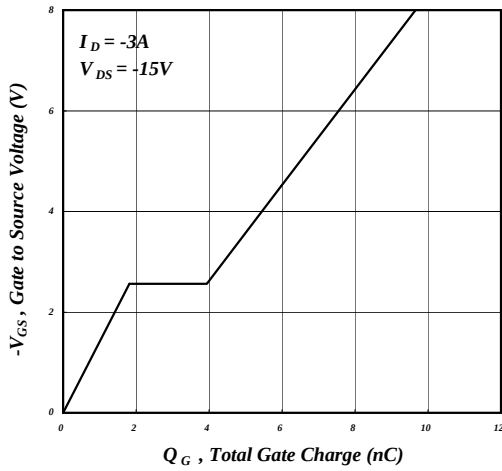


Fig 7. Gate Charge Characteristics

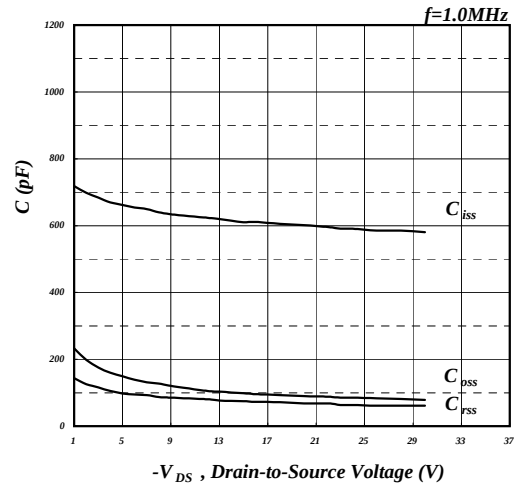


Fig 8. Typical Capacitance Characteristics

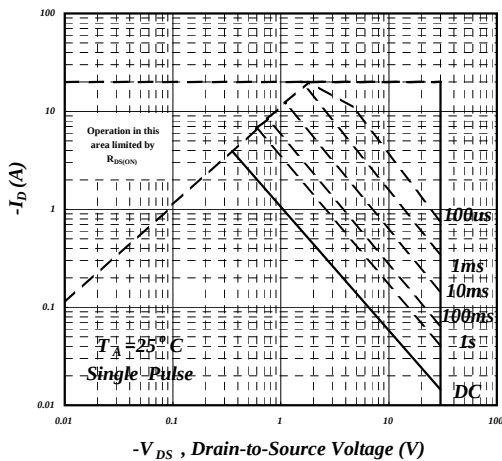


Fig 9. Maximum Safe Operating Area

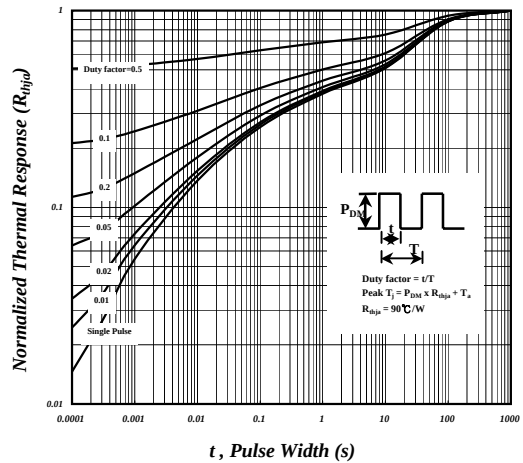


Fig 10. Effective Transient Thermal Impedance

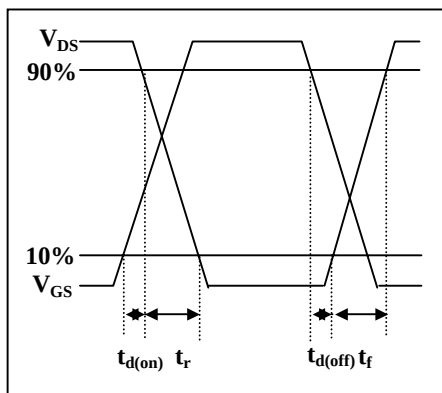


Fig 11. Switching Time Waveform

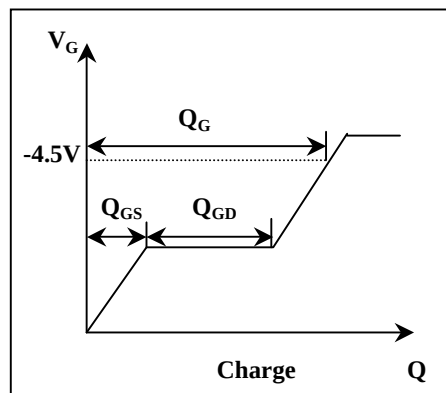
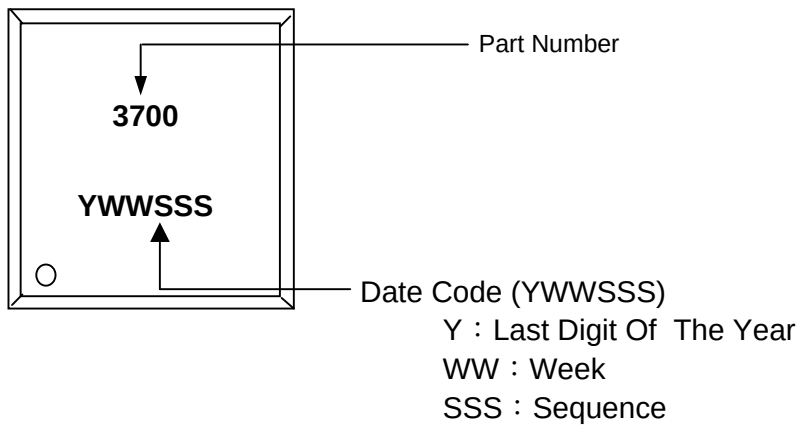
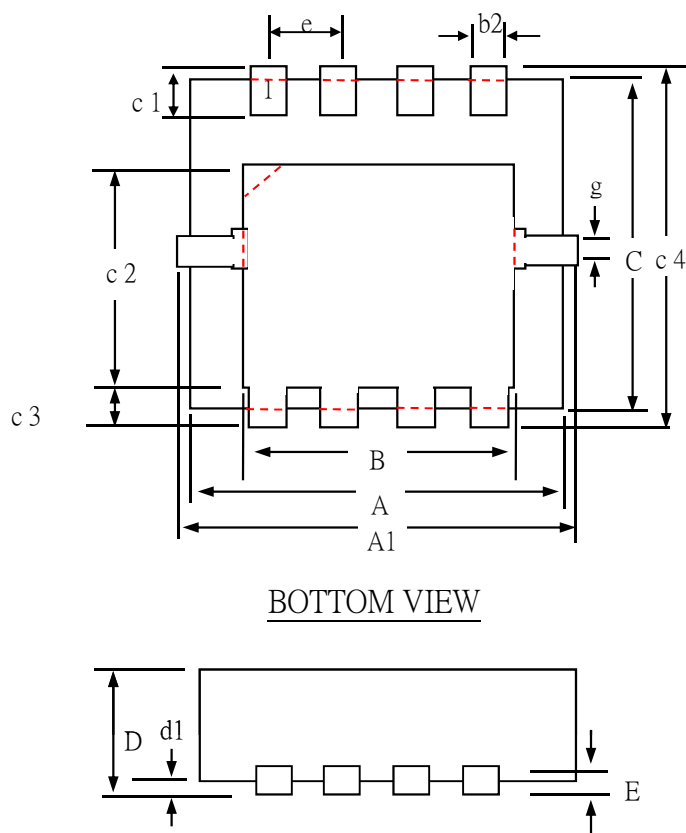


Fig 12. Gate Charge Waveform

MARKING INFORMATION

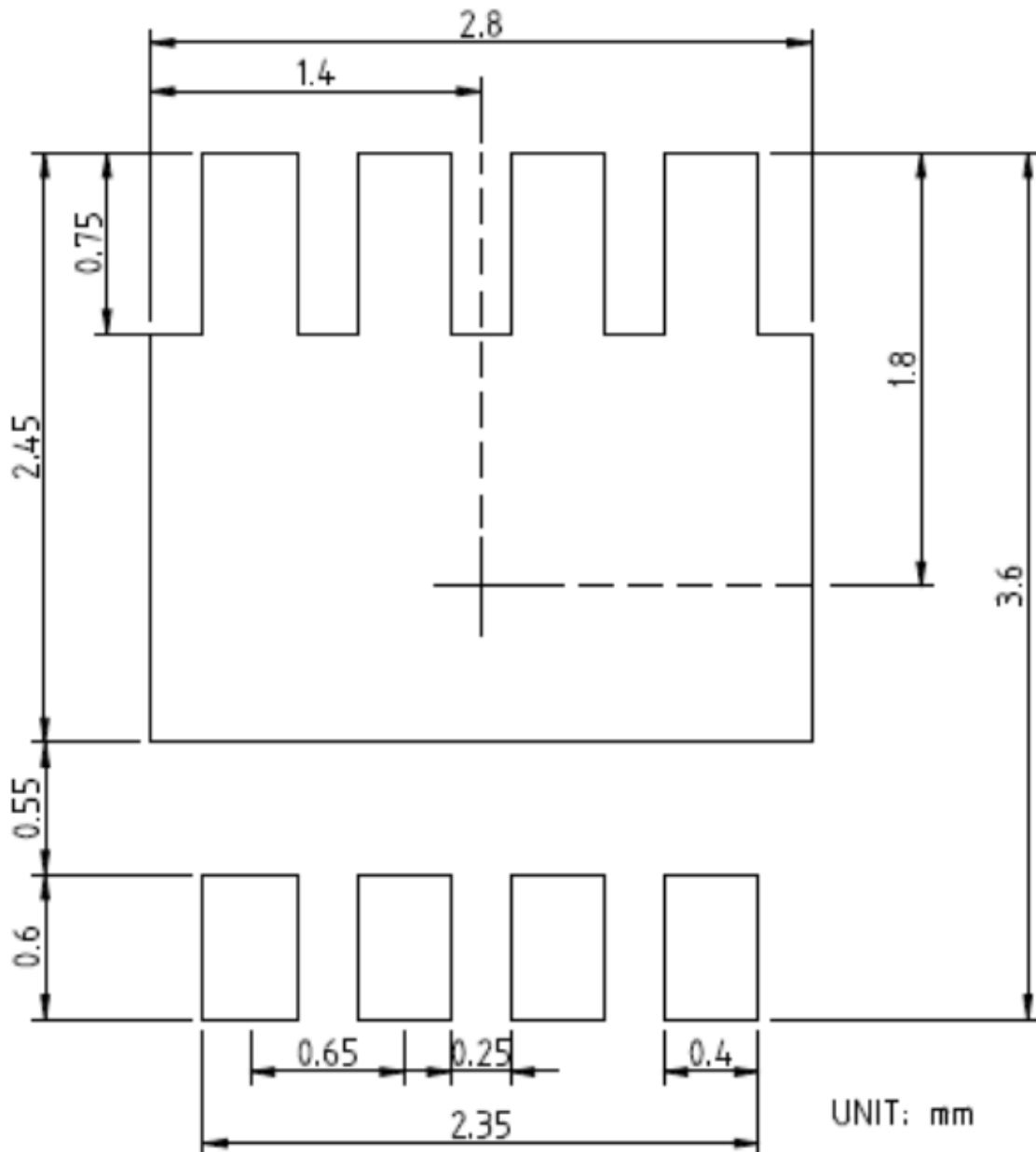
Package Outline : PMPAK 3x3



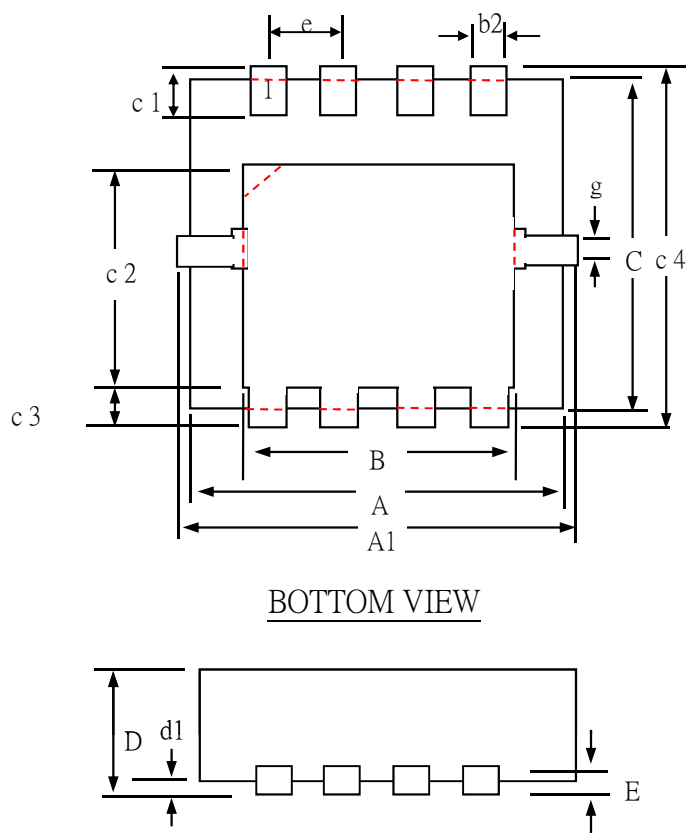
SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.90	3.10	3.40
B	2.20	2.45	2.80
e	0.60	0.65	0.70
b2	0.20	0.30	0.40
C	2.90	3.10	3.40
c1	0.10	0.30	0.50
c2	1.20	1.70	2.20
c3	0.10	0.38	0.65
D	0.65	0.80	1.05
d1	0.00	0.10	0.20
E	0.10	0.18	0.25
A1	2.900	3.30	3.600
c4	2.900	3.30	3.600
g	0.20 (ref)		

- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.

PMPAK3X3 FOOTPRINT :



Package Outline : PMPAK 3x3



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.90	3.10	3.40
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e	0.60	0.65	0.70
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c2	1.20	1.70	2.20
c3	0.10	0.38	0.65
D	0.65	0.80	1.05
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E	0.10	0.18	0.25
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- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
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PMPAK3X3 FOOTPRINT :

